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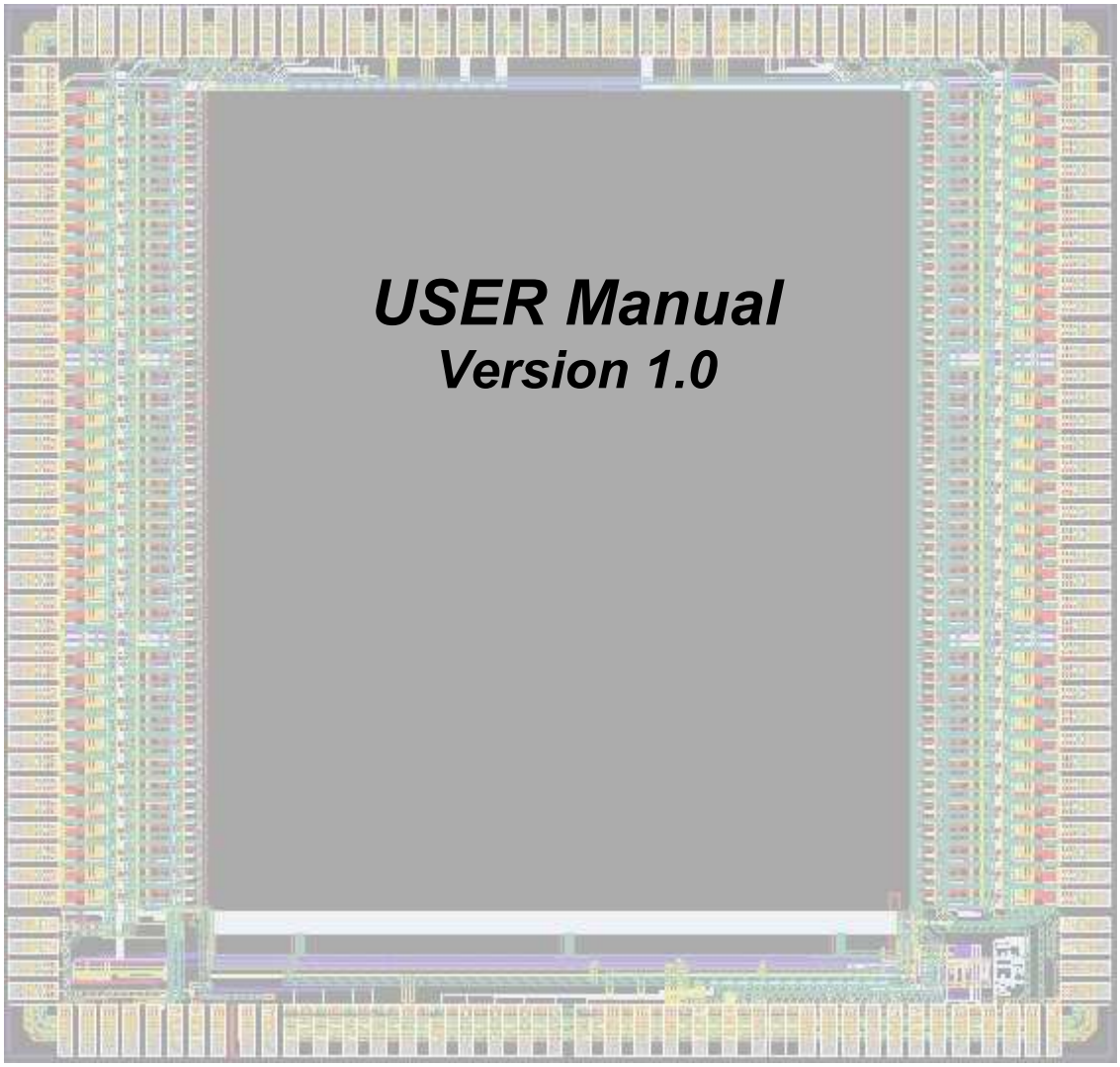
AFTER Asic



USER Manual
Version 1.0

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Date: April 2008

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1 Introduction

The ***AFTER*** (**A**sic **F**or **T**PC **E**lectronic **R**ead out) chip is designed to process the signals coming out from the (MICROMEGAS) end-caps of the T2K **T**ime **P**rojection **C**hamber detector. The front-end electronics of these detectors (Fig 1) is split into two types of boards: ***FEC*** & ***FEM***.

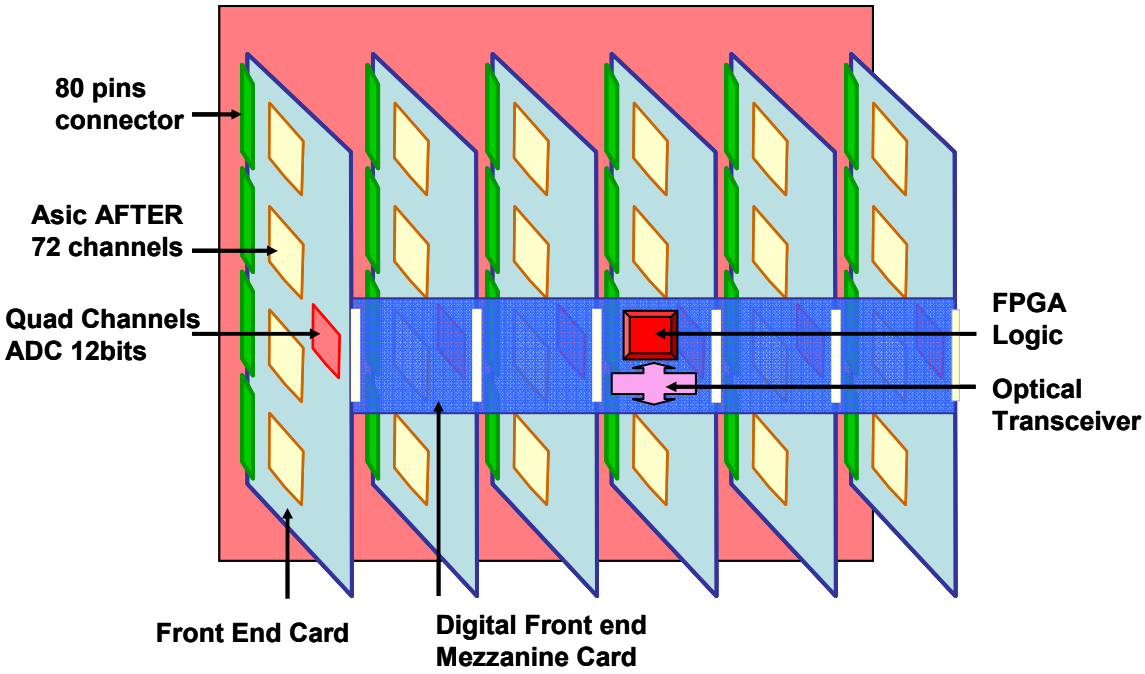


Fig 1: Front end electronics of a TPC end-cap module.

F.E.C (**F**ront end **E**lectronic **C**ard): This card includes 4 AFTER chips together with a quad-channel ADC. This card is plugged directly on the TPC end-cap module through 4 connectors, each connecting the 72 inputs of one AFTER chip to the detector. The analog output of the AFTER chip is digitized by one of the 4 ADC channels of the FEC. The 4 ADC outputs are sent to the FEM through a single output connector. The FEC behaves like a slave device controlled by the FEM. A total of 6 FEC, controlled by a single FEM are required to read one TPC Micromegas module.

F.E.M (**F**ront **E**nd **M**ezzanine): This card controls the 6 FECs of a TPC end-cap module. Each FEC is connected to a FEM by a single connector that provides the main communication signals between the two cards. Some of them have critical timings and make use of LVDS levels, as serial frames coming out from the ADC (up to 120 MHz DDR) and ADC and SCA clocks. The other less critical signals as slow control and SCA signals are transmitted using CMOS levels

The FEM output data is transmitted to the Digital Concentrator Card, outside of the magnet, through an Optical Transceiver.

1.1 *AFTER General Description.*

The ***AFTER*** chip includes **72** channels (Fig 2) handling each one detector pad. A channel integrates mainly: a charge sensitive preamplifier, an analogue filter (shaper) and a 511-sample analog memory. This memory is based on a **S**witched **C**apacitor **A**rray structure (**SCA**), used as a circular buffer in which the analog signal coming out from the shaper is continuously sampled and stored. The sampling is stopped when an external Trigger arrives on the TPC **F**ront **E**nd **M**ezzanine (**F.E.M**). Then, the 511 samples of each channel are read back, starting by the oldest sample. The analogue data from all the channels are time domain multiplexed toward a single output to be sent to an external 12-bit ADC.

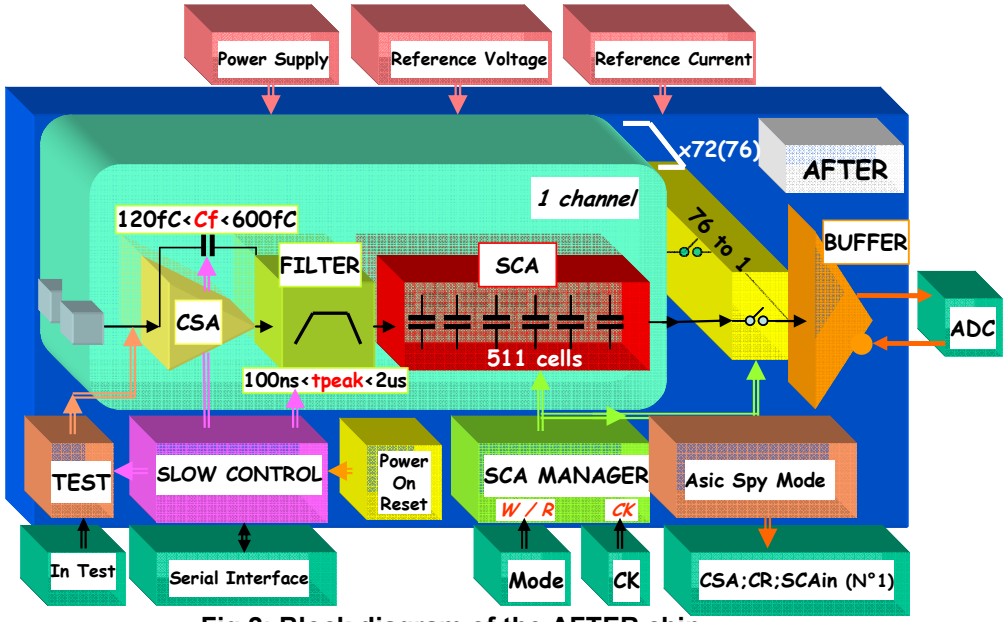


Fig 2: Block diagram of the AFTER chip.

The chip main parameters (gain, peaking time, test mode and asic control) are settable by Slow Control. Two chip inputs permit to calibrate or to test the 72 channels. A "spy" mode is available to control some internal test points (CSA & PZC outputs and SCA input) of the first analogue channel.

Table 1 gives the main specifications and requirements for the AFTER chip as defined in 2005.

Parameter	Value
Number of channels	*72*
Number of Time bins	*511*
MIP charge	*12fC to 60fC*
MIP/noise	*100*
Dynamic range	*10 MIPS on 12bits*
Dynamic range (output)	*2 V*
I.N.L	*1% range 0-3 MIPS; 5% range 3-10 MIPS*
Gain	*Adjustable (4 values)*
Sampling frequency	*1MHz to 50MHz*
Shaping Time	*100ns to 2μs*
Read out frequency	*20 to 25MHz*
Polarity of detector signal	*Negative (anode of TPC) or Positive (Cathode).*
Calibration	*Selection 1/72*
Test	*one internal test capacitor per channel*

Table 1: List of the AFTER chip requirements.

2 Architecture of the front-end part of the channel

The architecture of the front-end part has been optimized to match the noise requirements for the TPC and to deliver a shaped signal making possible to perform a precise TPC drift-time measurement. However, it takes also into account the power consumption and silicon area constraints. It can also fit various configurations of detector parameters (gain, capacitor and drift velocity…), and can deal with the both detector signal (positive or negative) polarities.

2.1 General description

The front-end channel (Fig 3) is made up of four stages:

- C.S.A: Charge Sensitive Amplifier
- PZC: the pole-zero cancellation stage
- R.C^2 filter: Sallen&Key filter
- An inverting 2 x Gain.

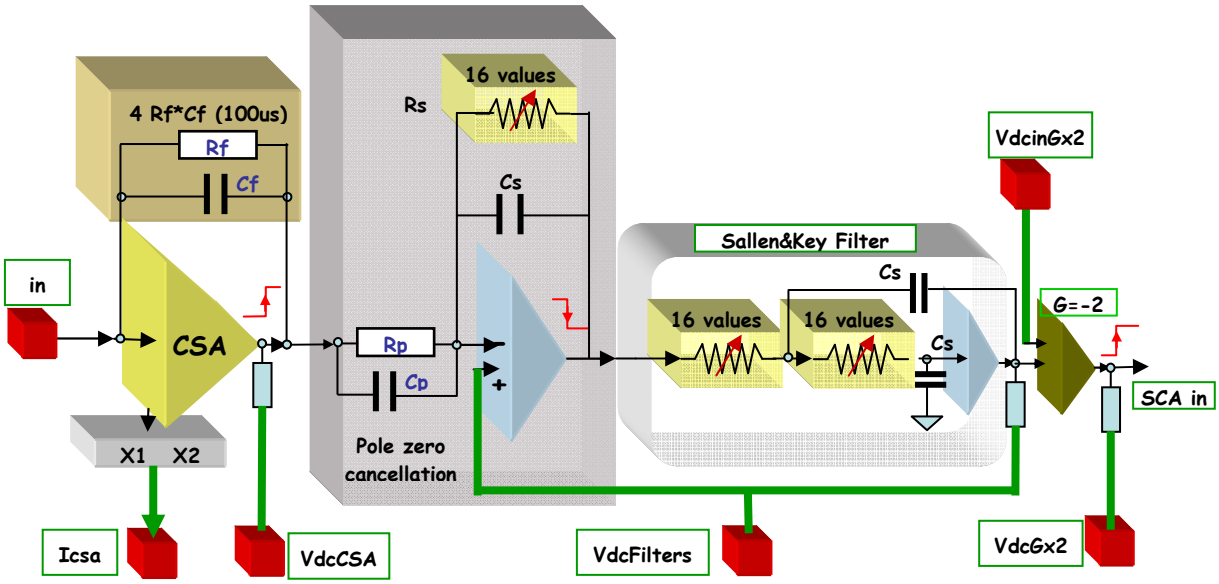


Fig 3: Schematic of the front-end part of the analog channel.

2.1.A The Charge Sensitive Amplifier

This amplifier is based on single-ended folded cascode architecture. The input transistor is a NMOS device and its drain current is defined and controlled on ***FEC*** through the pad **126** or **155**. It is optionally possible to increase this current by a factor of 2 via the slow control. This bias current choice (max 1mA) will be the result of a trade-off between the noise and power consumption performances that will depend on the application.
The CSA d.c. output voltage is defined also externally through the pad **133** & **148**. A fixed level of 2V allows the CSA to work with the both polarities of the input signal. The linear range of the CSA output voltage is **+/- 600mV**. The charge to voltage conversion is achieved by one of the four feedback capacitors selected by Slow Control. Their values are: **200fF**, **400fF**, **600f**F and **1pF** which are defining the four "ranges" of the chip (120fC, 240fC, 360fC and 600 fC).

The DC feedback of the CSA is achieved by an attenuating current conveyor (AICON). It is equivalent to a resistor and there are 4 possible values, each associated with one of the feedback capacitor to obtain a fixed time constant value of 100μs. **The maximum current that the CSA DC-feedback can source or sink to the detector is 5nA.**

2.1.B The pole-zero cancellation stage (PZC)

The PZC stage is used to avoid long duration undershoots at the shaped output. It introduces a zero to cancel the low frequency pole of the CSA and replaces it by a higher frequency pole. Its value is selectable, via Slow Control, between sixteen possible values (50ns to 1μs). The d.c. output voltage of this block is defined in external through the pad **134** & **147** and must be adapted to the polarity of the input signal. For the anode polarity (Micromegas of T2K), this reference voltage (2.2V) is set close to the positive rail so that its output can swing towards the negative rail. In the cathode configuration, the voltage must be tied to 0.7V.

2.1.C The RC^2 filter.

Associated with the previous PZC stage, this 2-complex pole Sallen-Key low pass filter provides a semi-Gaussian shaping of the analog channel. The filter damping factor is $\xi = 0.75$, so that the global filter response exhibits a 1% only undershoot.
The peaking time of the global filter is defined by switching different combination of resistors on both the PZC and filter stages. The available range of peaking time extends from **100ns** to **2μs** (**sixteen values**). The d.c. output voltage of the filter is defined as for the PZC (pin **134** & **147**), and must be adapted to the polarity of the input signal. In the TPC mode, this reference voltage (2.2V) is set close to the positive rail so that its output swings towards the negative rail. In the inverted configuration, this voltage must be set to 0.7V.

2.1.D The inverting x2 Gain.

This stage provides an extra x2 inverting voltage gain and the necessary buffering for the signal sampling in the SCA. Its total dynamic (full range) is 1.5V, mainly limited by slew rate effects. As it is an inverter stage, its d.c. output level voltage must be set close to the negative rail to deal with the positive swing of the signal (0.7V for T2K). This voltage is defined through the pads **135** & **146**. Its input common-mode voltage is defined by the pads **138** & **142**. These 2 pins are also used to supply the reference voltage of the SCA at a fixed value of 0.7V.

2.2 The Fixed Pattern Noise Channels (F.P.N)

A part of the SCA noise will be probably coherent between channels. To perform common mode rejection, 4 extra channels FPN (Fixed Pattern Noise) are included in the chip. The front-end part of these channels only includes the inverting 2x Gain stage for which the inputs have been connected to the input reference voltage. The F.P.N channels will be treated by the SCA exactly as the other channels. Off-line, their outputs can be subtracted to the 72 analog channels. This pseudo-differential operation is supposed to reject the major part of the coherent noise due to 2x Gain and SCA such as clock feed-through and couplings through the substrate. It also improves the power supplies rejection ratio (PSRR) of the chip.

These channels are distributed uniformly in the chip as shown on Fig 11 . Their readout indexes are: 13, 26, 51 & 64.

2.3 The "integrator" mode.

A new functionality has been integrated in the production version of the chip. It will be possible to program the shaping time of the PZC stage to 1µs value independently of the 16 possible shaping time values of the Sallen-Key filter. This request comes from another project for which the double pulse resolution is important. This mode will be validated by programming the bit 2^9 of the slow control register number 1.

3 Architecture of the SCA

The analog memory is based on the **S**witched **C**apacitor **A**rray structure. It is used as a 511 cell-depth circular buffer in which the analog signal coming out from the front-end analog channel is continuously sampled and stored at a sampling rate **Fs**. The sampler is stopped on the trailing edge of the **write** signal of the chip that is generated by the ***FEM*** after the reception of the external **TRIGGER** signal. Then for each channel, all or one part of the 511 samples are read back, starting by the oldest sample. The analog data coming from the 76 channels are time-domain multiplexed and read toward a single external 12-bit ADC channel.

3.1 General description

The Switch Capacitor Array includes 76 channels of each 511 capacitor cells. The 511 cells of a channel are arranged in line. All the capacitors of a line are sharing the same input analogue and reference busses and the same read top and bottom busses connected to a read amplifier. All the cells of the 76 channels with the same index (namely a column) are sharing the same write and read column signals. It means that all the cells of a column are written or read at the same time. The write and read operations are performed successively.

3.2 Description of the Write and Read SCA operations.

The SCA uses 4 digital command signals.

- Two clocks sequencing the write and read operations:
  - **Wck** : the write clock; **Rck** : the read clock.

These clocks are active on their rising edges, and may be interrupted when they are not used.

- Two frame signals defining the write and read operations (Fig **4**):
  - **Write**: defining the write operation; **Read**: defining the read operation.

These two signals should not overlap and are active on their high levels. The clock signals are provided using differential LVDS levels. The write and read signals are received in CMOS levels.

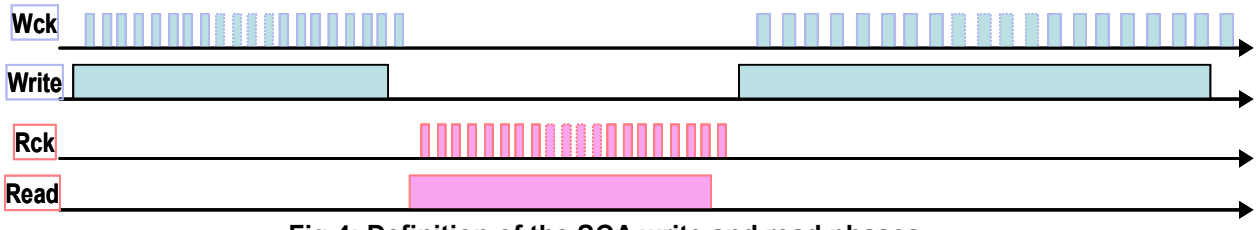


Fig 4: Definition of the SCA write and read phases.

3.2.A The SCA Write phase

The write operation starts when the ***Write*** signal is set to 1. Its positive edge asynchronously resets the write pointer to the column 0. This pointer is then shifted to the successive columns on the rising edge of ***Wck***, performing the writing operation. When ***Write*** comes back to 0, the write pointer position is frozen and the writing operation is stopped.
The ***Write*** signal can be set or reset asynchronously with the clock, but in this case the write operation on the last cell may be incomplete. So it is better to change the state of the ***Write*** signal on the negative transition of ***Wck.***
To complete the write operation, at least one ***Wck*** positive edge is required after the ***Write*** signal falling edge.

3.2.B The SCA Read phase

The read operation is initiated when the ***Read*** signal is set to 1.
Its positive edge asynchronously copies the write pointer to the read pointer and reset the multiplexer register. As long as Read stays to 1, the analogue signals are sequentially multiplexed to the output at each rising edge of the ***Rck***. The first column read is the one following the last written. To read a column, 79 ***Rck*** periods are needed (Fig 5). The 3 first output samples are corresponding to 3 "reset level" defined in 3.2.C. The 76 following are corresponding to the analogue data stored in the different lines of the column starting from line 1 and multiplexed alternately from group 0 and group 1. After the last (76th) cell of this column, the read pointer is shifted and the same operation is performed on the next column.

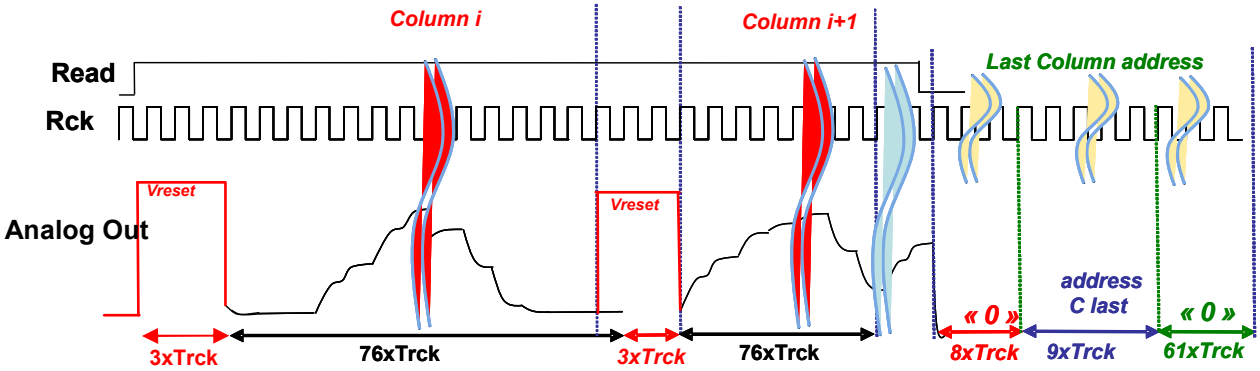


Fig 5: Chronogram of the SCA Read phase.

When ***Read*** comes back to 0, this sequence is asynchronously interrupted and the current address of the read pointer is encoded and multiplexed to the output. The negative ***Read*** transition can occur whenever the controller decides it. This permits to read a limited number of cells.
This operation is then finished. It is also interrupted when ***Write*** is set to 1.
As for Write, it could be convenient to set or reset the ***Read*** signal on the negative edge of ***Rck***.
The read sequence order of the 76 channels is summarized in the Table 2.

Readout Index	Channel index	Pin Number of the channel input	Readout Index	Channel index	Pin Number of the channel input
1	Reset1				
2	Reset2				
3	Reset3				
4	1	36	42	37	120
5	2	35	43	38	119
6	3	34	44	39	118
7	4	33	45	40	117
8	5	32	46	41	116
9	6	31	47	42	115
10	7	30	48	43	114
11	8	29	49	44	113
12	9	28	50	45	112
13	10	27	51	46	111
14	11	26	52	47	110
15	12	25	53	48	109
16	FPN1		54	FPN3	
17	13	24	55	49	108
18	14	23	56	50	107
19	15	22	57	51	106
20	16	21	58	52	105
21	17	20	59	53	104
22	18	19	60	54	103
23	19	18	61	55	102
24	20	17	62	56	101
25	21	16	63	57	100
26	22	15	64	58	99
27	23	14	65	59	98
28	24	13	66	60	97
29	FPN2		67	FPN4	
30	25	12	68	61	96
31	26	11	69	62	95
32	27	10	70	63	94
33	28	9	71	64	93
34	29	8	72	65	92
35	30	7	73	66	91
36	31	6	74	67	90
37	32	5	75	68	89
38	33	4	76	69	88
39	34	3	77	70	87
40	35	2	78	71	86
41	36	1	79	72	85

Table 2: Description of data readout frame.

3.2.C Definition of the "Reset states"

The three consecutive so-called reset states are corresponding to the SCA output states when a write operation is performed in the SCA or when the read operation of a column is started. These states can be used for debugging or testing purpose.

The first reset state corresponds to the phase during which the read-amplifier is reset (start of column read or write operation). During this phase, the read-amplifier output goes to vdd, but the multiplexer output state depends on configuration of the bits 6 and 7 of register 2. If bit 6 is set to 0, the reference voltage used to define the x2 gain stage output voltage (Vdc_g2d) is multiplexed toward the chip output. It can be used to measure the noise of the AFTER output stages (buffer of the multiplexer + differential output buffer). If bit 6 is set to 1, a digital voltage, defined by the bit 7 is multiplexed toward the output. This can be used as marker to check the synchronisation of the ADC output data.

During the second reset state, the channel 1 output is multiplexed toward to the output while the capacitor to read is placed across the read amplifier. So the output signal first increases in the direction of vdd during ~10 ns corresponding to the settling times of the mux and the output buffer. Once the mux output has reached the read amplifier output voltage, the output follows the output of the read amplifier settling towards its final value.

During the third reset state, the chip output voltage corresponds to the Vdc_g2d voltage sampled on the analogue bus of the multiplexer.

3.2.D Reading the last read cell index.

After the ***READ*** signal comes back to 0, a special frame, coding the physical index of the last read cell, is sent to the chip output. This serial frame use binary levels which are clamped internally in the chip by the multiplexer and the output buffer. To recover the digital levels, the user can keep the state of the ADC MSB only. The frame is build as following:

- 8 binary low levels.
- the 9 bits coding the last read cell index sent serially (MSB first).
- 61 binary low levels.

At the end of this operation, the analogue output comes back to the reset level of the read amplifier of channel 1.

The last read cell information can be used to check the synchronisation between SCA chips or to correct data from physical fix pattern noise (i.e. pedestal dependency with the physical index of the SCA cell).

If the bit#4 of the register#2 is set to 1, the control word "101011001" is sent instead the last read cell address for debugging purpose.

In the prototype of the AFTER chip, there is a mistake in the design of the block performing the encoding of this last read cell. This will be corrected for the production of the chip. Nevertheless, the effect of this error is only a permutation between codes and can be easily corrected by the following algorithm (a Labview program performing this correction is given in Annexe 2):

If the cell index is <= 255 => no encoding problem.
Else it must be re-encoded as following:
In Last_cell<8:0> where last_cell<8> is the MSB:
the Nibble Last_cell<7:4> must be replaced by its complement to 1

3.2.E Timing requirements for the SCA signals.

Table 3 summarizes the requirements for the digital signals driven the SCA.

Name	Description	Min	Typ.	Max
F *Wck*	frequency of ***Wck***	0	50MHz	100MHz
F *Wck* jitter	Jitter of ***Wck***		50 ps rms	100ps rms
F *Wck* _cycle	Duty cycle of ***Wck***	0.25	0.5	0.75
t *Wck* to Fw	Time between a ***Write*** transition and positive edge of ***Wck***	5ns		
t *Wck* to Write	Time between positive edge of ***Wck*** and a ***Write*** transition.	5ns		
t *Wck* to sample	Time between positive edge of ***Wck*** and the sample operation		3ns	
F *Rck*	frequency of ***Rck***	0		25 MHz
***Rck* jitter**	Jitter of ***Rck***			100ps rms
***Rck* _cycle**	Duty cycle of ***Rck***	0.25	0.5	0.75
t Read to *Rck*	Time between a ***Read*** transition and positive edge of ***Rck***	5ns		
t *Rck* to Read	Time between positive edge of ***Rck*** and a ***Read*** transition.	5ns		
t *Rck* to Multiplex	Time between positive edge of ***Rck*** and the effective multiplexing		6ns	
tr multiplex	Stabilization time of the analog signal at the multiplexer output		35 ns	

Table 3: Specifications for the timing of the digital signals used in the SCA.

4 The Differential Output Buffer

This buffer is designed to drive differentially the external 12-bit ADC (AD9229) at up to 20 MHz readout frequency. Its input, connected to the SCA multiplexer output is single-ended while its output is differential. As shown on Fig 6, the single-ended to differential conversion is achieved using a full differential amplifier with its negative input connected to a reference voltage **Vicm** This buffer also provides a gain of 1.328 between the differential output ($\mathbf{V_{op}}$-$\mathbf{V_{on}}$) and its input ($\mathbf{V_{ip}}$) to fit with the differential ADC input range (**+/-1 V**). Thanks an internal common mode feedback, the common mode output voltage of the amplifier (($\mathbf{V_{op}}$+$\mathbf{V_{on}}$)/2) is equal to the voltage applied on the ***vocm*** (Pin 68) input. Its standard value is ***VddADC/2*** = 1.65V.
The **Vicm** (pin 71) external input voltage permits to adjust the input range of the buffer. To optimize it, this voltage must be set to a voltage equal to the peak voltage of a pulse corresponding to half the chip dynamic range:

$Vicm=[Vdc_{SCA\ output}$+/- $Vpeak_{SCA\ output}]/2$ (+ for anode mode, - for the cathode one)

The buffer has to deal with the ADC input architecture and the parasitic elements due to interconnection on the ***FEC.*** It is designed to have a 1/1000 settling time smaller than 25ns corresponding to half the ADC clock period.

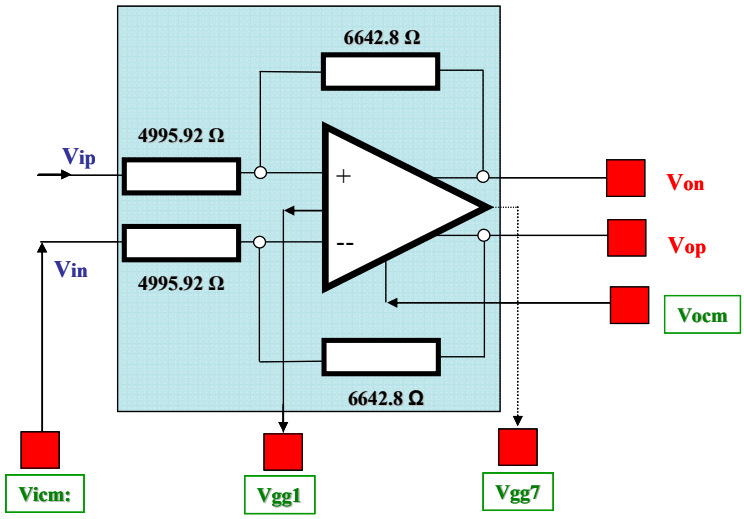


Fig 6: Schematic of the readout buffer.

5 Architecture of the Test system & "spy" mode

The AFTER chip includes a test system useful for: electrical calibration, asic test bench and functionality control of all electronic channels (Asic to acquisition board). The chip also offers the possibility to spy 3 critical signals of the front-end part of analogue channel number 1: CSA, PZC and Gain-2 outputs.

5.1 General description of the test system

The AFTER asic offers 3 different modes of test: calibration, test and functionality.

The Calibration operation consists in generating the same charge on the inputs of all the channels of all the asics of a given FEC or of all the FEC of a TPC readout plan. Therefore, the charge pulse is generated outside of the chip, directly on the FEC. The charge injection is generated by applying a voltage step to a precision capacitor connected to the input of the selected channel via the ***In_cal*** input (pin 39).

The channel selection is made by switches inside the chip configured by slow control (Fig 7).

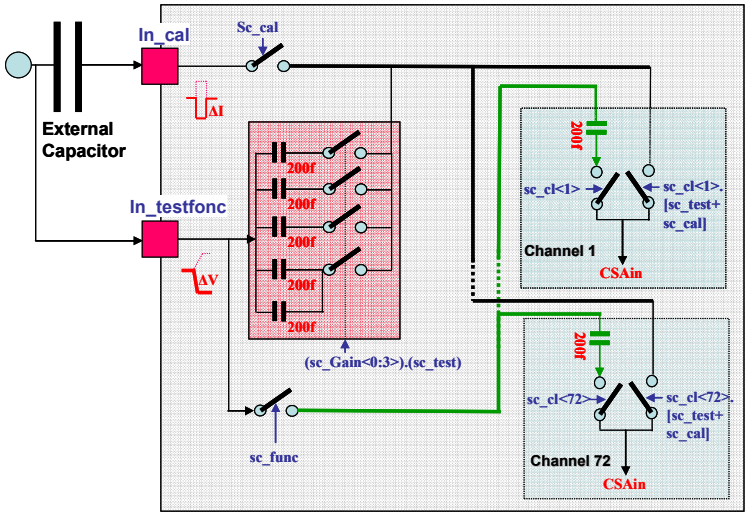


Fig 7: Schematic of the test system

For the two other modes, the charge injection is generated through internal capacitors driven by an externally generated voltage applied on the pad ***In_testfonc*** (pin 40).

In the test mode, four different values of injection capacitor, one for each charge range, are used. This permits working with the same test voltage pulse level for the 4 ranges. The selection of the injection capacitor is automatically done when the charge range is selected.

In the functionality test mode, a single capacitor (200fF) per channel is used.

For all the 3 test modes, the selection of the tested channel is made via slow control.

For the two first modes, only one tested channel must be selected whereas up to the 76 channels can be selected when the functionality mode is used.

For the FPN channel, only the functionality test is usable. In this case, the input voltage step is applied directly to the input of the inverting 2x GAIN stage of the selected FPN channel.

5.2 General description of the "spy" mode

This mode permits to visualize on an oscilloscope the outputs of the CSA, PZC block and Gain-2 of the channel number 1. This feature will be useful to compare experimental and simulation results. By slow control, one of these 3 signals (Fig 8) can be multiplexed, through an internal buffer, to the pad ***Out_debug*** (pin 46). If the "spy" mode is not selected, the internal buffers are put in a standby mode.

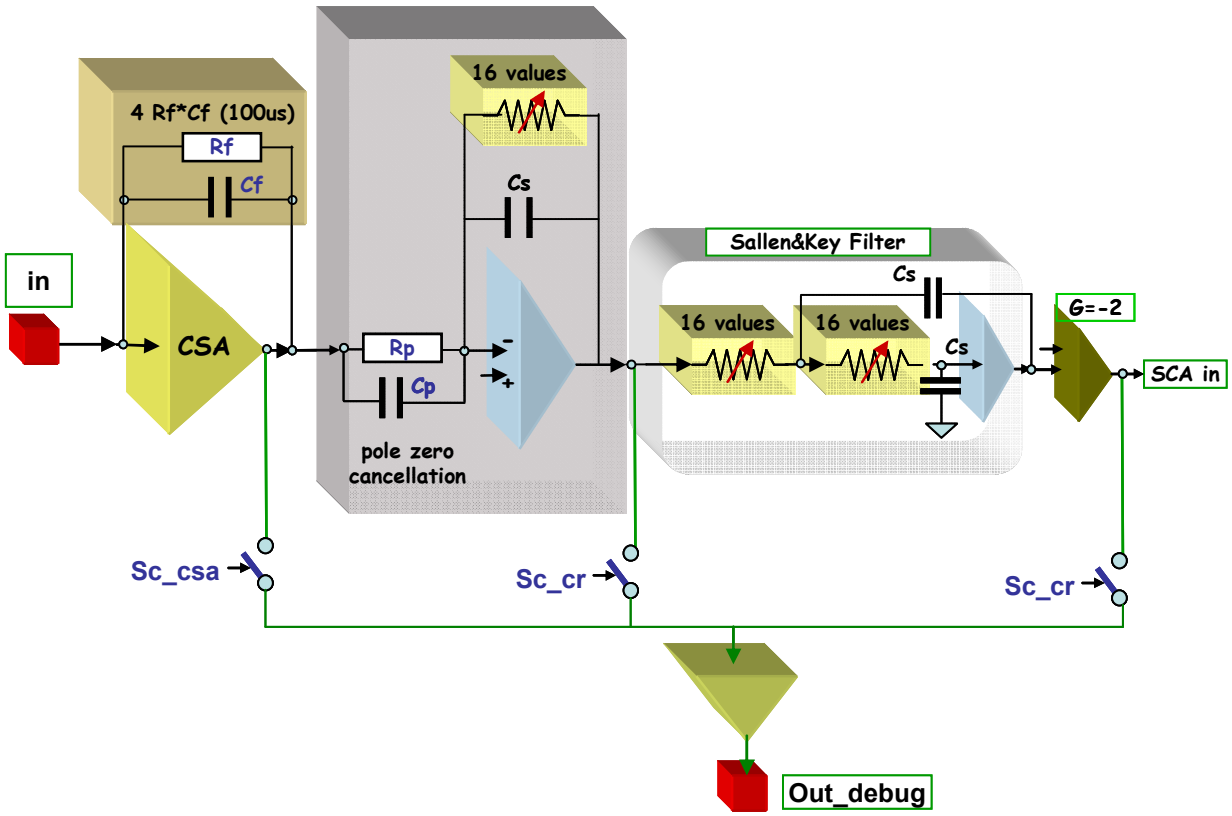


Fig 8: Schematic of the "spy" mode.

6 The Slow Control

The slow control permits to program various chip parameters (gain, shaping time, test mode …) and to access to specific modes of operation. It is a serial protocol, used in several ASICs designed in DAPNIA laboratory. It gives access in write or read mode to the four internal registers of the chip:

- 2 configuration registers: 16-bit wide.
- 2 channels selection registers: 38-bits wide.

6.1 Power on Reset

When the chip is powered on, an internal “power on reset” device delivers a reset pulse (about 1ms of duration) resetting the 4 registers (all bits to 0)

6.2 Description of the slow-control serial link.

The link uses **4** signals. They all use **CMOS** [0V; 3.3V] level:

- ***Sc_din [pin N°51]***: input data of the serial link.
- ***Sc_ck [pin N°53]***: clock of the serial link.
- ***Sc_en [pin N°52]***: enable of the serial link.
- ***Sc_dout [pin N° 54]***: output data of the serial link.

The signals ***Sc_din*** & ***Sc_en*** must be synchronous to the rising edge of ***Sc_ck.*** The data are sampled on the input lines, decoded and operations of reading/writing are carried out, by the asic, on the falling edge of ***Sc_ck***. Thus, the data at the output of ***Sc_dout*** will be synchronous on this edge.
On ***Sc_din,*** the data frame is defined as:

[r/wb] [Ad6… Ad0] [DNBD-1…D0]

[**r/wb**]: This first bit defines the type of operation. **r/wb** =1 : readout; 0: write.
[**Ad6… Ad0**]: These 7 bits give the address of the target register.
[**DNBD-1…D0**]: This is the **NBD** bits of data to transmit.

The most significant bit of the address and the data is always sent (or read) first.
The ***Sc_en*** signal frames the data sent on ***Sc_din***. It must go up simultaneously with the positioning of [**r/wb**] and must go down one cycle of ***Sc_ck*** after the positioning of the last bit of data (***D0***) on ***Sc_din***. Thus, the data packet defined by the setting of the ***Sc_en*** signal to 1 must frame [***8+ NBD*** falling edges**]** of ***Sc_ck***.
The ***Sc_ck*** clock must be present immediately after the beginning of the data frame and must continue at least during three clocks (falling edge) after the falling edge of ***Sc_en***. After that, it is better to stop it (its idle state can be high or low).

Between the slow-control frames, the ***Sc_dout*** output is in idle state. If the ***force_eout*** bit of the register 2 is high, this output keeps its last valid value. If it is low (default mode), the output is in high impedance state.

6.3 *Resynchronisation of Sc_dout.*

All the data on the ***Sc_dout*** line are, by default, locally synchronised on the ***Sc_ck*** falling edge. But this synchronising is partially lost due to the different transit times in the chip. It is also possible, by slow control, to synchronise the signal on ***Sc_dout***. This is done by the bit 9 (***out_resync***) of the register 2, and the choice of active edge by the bit 10 (***synchro_inv***). If the state is "1", the synchronisation will be made on the falling edge of ***Sc_ck***; "0" on the rising edge. All the chronograms on the next figures are in the case where the slowcontrol bit ***out_resync*** is "0".

6.4 *Writing mode (address other that 0) in a register of C bits.*

The write mode (Fig 9) is defined by the first bit **r/wb = 0**. The falling edge of ***Sc_en*** starts the writing of the **C** last bits on ***Sc_din*** in the target register. After the eighth falling edge of ***Sc_ck***, ***Sc_dout*** leaves its idle state. During **C** clocks, ***Sc_dout*** takes the **Y<n :1>** states, according to the history on the **Sc_din** line. Then, it will take the states present **C** clocks before (A<0>, D<15>, D<14> in the normal case where C=NBD).

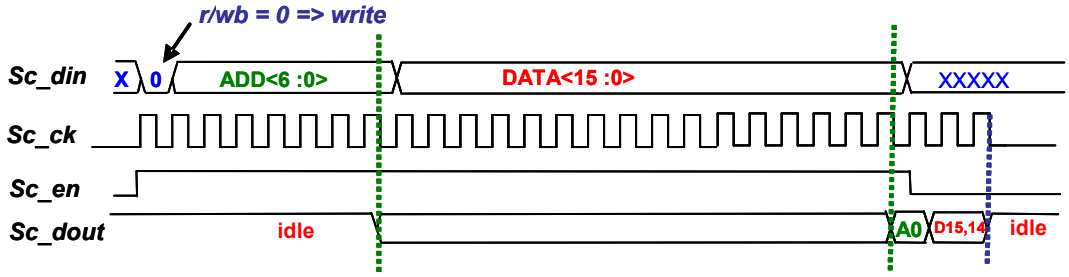


Fig 9: Operation of a Slow-control Write operation.

Sc_dout will come back to its idle state 3 rising edges of the clock after the falling of ***Sc_en.*** The number of **NBD** bits present in the data part of ***Sc_din*** can be greater than the size of the register (**C** bits). In this case, only the **C** last bits will be written in the register. The **NBD-C-2** first bits of the data will go out on the ***Sc_dout*** after A0, D15 & D14. This feature can be used to test the serial link.

6.5 *Case of Register 0.*

The register **0** doesn't physically exist. But, when it is addressed in write mode, ***Sc_dout*** recopy the data on ***Sc_din*** (after the eighth falling edge of ***Sc_ck***). ***Sc_dout*** comes back to the idle state (3 rising edges after the falling edge of ***Sc_en***).

6.6 *Read operation on a C bits Register.*

In the readout mode (Fig 10), ***Sc_en*** must cover more than **8+C-2** falling edges of ***Sc_ck***. A minimum of 3 falling edges of ***Sc_ck*** after the falling of ***Sc_en***, is necessary to finish the reading phase.

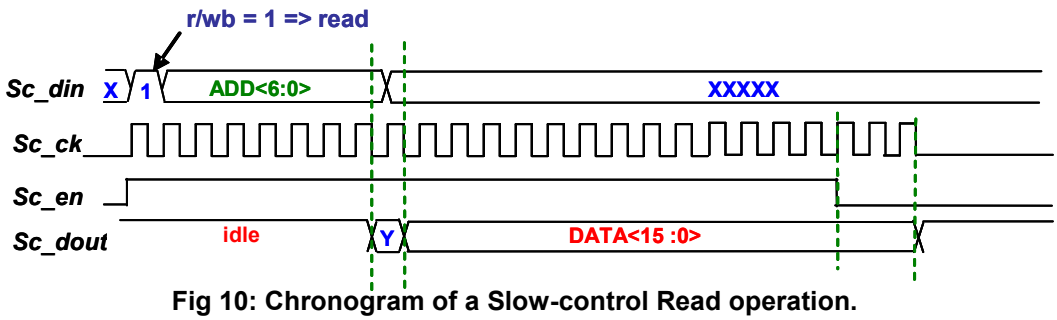


Fig 10: Chronogram of a Slow-control Read operation.

The first bit on ***Sc_din*** must be to “1” (**r/wb**)**.** Thus the 7 other bits define the address of the register. The next bits can be indefinite.
At the eighth falling edge of ***Sc_ck***, the address is decoded and ***Sc_dout*** leaves the idle state. During 1 clock cycle, its state **Y** depends on history of the serial link.
At the ninth falling edge of ***Sc_ck***, the data of the register is serialized toward ***Sc_dout*** during **C** clock cycles. After these **C** clock cycles, the data coming out from the ***Sc_dout*** are no more valid.
As for the writing phase, ***Sc_dout*** go back to the idle state, **3** clock cycles after the falling edge of ***Sc_en.***

6.7 Timing specifications for the AFTER slow-control serial link.

The timing specifications for the slow-control link are summarized in Table 4.

Name	Description	Min	Typ	Max
F Sc_ck	Slow control clock frequency	*0*		30MHz
tH_Sc_ck, tL_Sc_ck	Slow control clock minimum duration at “1” (or “0”) state	*10ns*		
t Sc_en* to *Sc_ck	delay between SC_en transition & rising edge of Sc_ck	*10ns*		
t Sc_din* to *Sc_ck	delay between SC_din transition & rising edge of Sc_ck	*10ns*		15ns
t Sc_ck* to *Sc_dout	delay between rising edge of Sc_ck & Sc_dout transition	*10ns*		

Table 4: Timing specifications for the slow-control.

6.8 Description of the registers.

The AFTER chip includes 4 control registers; two 16-bit wide and two of 38-bits wide. Their mapping (also including the dummy register of address 0 and asic version number register of address 6) is given in Table 5.

Address	name	width	access	action
0	**Dummy**		W	used to test the serial link (cf 6.5)
1	**Configuration 1**	16 bits	R/W	chip configuration
2	**Configuration 2**	16 bits	R/W	special modes and test config.
3	**Injection 1**	38 bits	R/W	selection of tested channels
4	**Injection 2**	38 bits	R/W	selection of tested channels
6	**Version number**	16 bits	R	Contains the version number of the chip

Table 5: Mapping of the AFTER slow-control registers.

6.8.A Configuration Register 1.

This 16-bit register is located at address number 1 (Table 6). Its 9 first bits are defining the configuration for the analog part of the channel before the SCA. The last 3 bits allow controlling the chip power consumption.

bit	name	action
0	**Icsa**	if 1, the nominal CSA bias current is x2
1	**Gain0**	LSB of the gain tuning
2	**Gain1**	MSB of the gain tuning
3	**Time0**	LSB of the filter peaking time
4	**Time1**	bit 1 of the filter peaking time
5	**Time2**	bit 2 of the filter peaking time

6	**Time3**	MSB of the filter peaking time
7	**Test0**	LSB of the test mode register
8	**Test1**	MSB of the test mode register
9	**Integrator mode**	If 1, set the PZC shaping time value to 1µs (only in production version)
10		
11		
12		
13	**power_down_write**	if 1, put the write section in power down mode
14	**power_down_read**	if 1 put the read section in power down mode
15	**alternate_power**	if 1, set alternatively the read and write sections in power down mode.

Table 6: Description of the configuration Register 1.

- ***bit Gain0 to Gain1:***

These 2 bits are defining the input charge range. This range is made by selecting one feedback capacitor among 4 on the C.S.A (Table 7).

Gain1	Gain0	Charge Range
0	**0**	***120fC***
0	**1**	***240fC***
1	**0**	***360fC***
1	**1**	***600fC***

Table 7: Definition of the dynamic range.

- ***bit Time0 to Time3:***

These 4 bits are setting the peaking time of the shaper (Table 8), by switching resistors on the PZC & SK filter.

Time3	Time2	Time1	Time0	Peaking Time [5%_100%] (ns)
0	**0**	**0**	**0**	***116***
0	**0**	**0**	**1**	***200***
0	**0**	**1**	**0**	***412***
0	**0**	**1**	**1**	***505***
0	**1**	**0**	**0**	***610***
0	**1**	**0**	**1**	***695***
0	**1**	**1**	**0**	***912***
0	**1**	**1**	**1**	***993***
1	**0**	**0**	**0**	***1054***
1	**0**	**0**	**1**	***1134***
1	**0**	**1**	**0**	***1343***
1	**0**	**1**	**1**	***1421***
1	**1**	**0**	**0**	***1546***
1	**1**	**0**	**1**	***1626***
1	**1**	**1**	**0**	***1834***
1	**1**	**1**	**1**	***1912***

Table 8: Definition of the peaking time.

- ***bit Test0 to Test1:***

These bits are defining the test modes (Table 9).

Test1	Test0	Test mode
0	**0**	***nothing***
0	**1**	***calibration***
1	**0**	***test***
1	**1**	***functionality***

Table 9: Definition of the test modes.

The calibration, test & functionality tests require the choice of one or several channels. This is done by the registers 3 & 4.

- ***bit* integrator mode.**

This bit fixes the shaping time of the PZC stage to 1µs value independently of the 16 possible shaping time values of the Sallen-Key filter.

- ***bits* power_down_write, power_down_read & alternate_power.**

These bits give the possibility to manage the power consumption by the fact that when the chip is in the write mode, the reading part is not used and therefore the SCA line buffer can be put in a standby mode. In the read mode, as the analog data is stored in the SCA, the writing part of the analog channel (pole-zero cancellation stage, Sallen&Key filter and Gain-2) can be put also in a standby mode. This functional mode is activated by the bit ***alternate_power***. It is also possible to force independently the writing and the reading parts in a standby mode by the bits ***power_down_write*** and ***power_down_read***.

6.8.B Configuration Register 2

This 16-bit register located at address n°2. It is used to test and the control of the SCA reading (Table 10).

bit	name	action
0	**debug0**	LSB of the debug mode register
1	**debug1**	MSB of the debug mode register
2		
3	**read_from_0**	if 1, force to start the readout from column 0
4	**test_digout**	if 1, a test pattern is serialized to the output instead of the 9bit address of the last read column
5	**set_l0_when_rst**	Not used. Must be set to 0
6	**en_mker_rst**	if 1, a "digital" marker (near gnd or vdd levels) is multiplexed to the analog output during "reset operation"
7	**rst_lv_to 1**	set the level of the digital marker (when en_mker_rst=1)
8	**boost_pw**	If 1, the output current of the analog block Gain-2 is increased (+20%)
9	**out_resync**	If 1, the SC output data is resynchronized by a clock edge (selected by synchro_inv)
10	**synchro_inv**	select the edge for the synchronizing of the SC output data (0= rising, 1=falling)
11	**force_eout**	If 1, inhibit the 3rd state functionality of the SC output buffer.
12	**Cur_RA<0>**	These 2 bits manage the current of the SCA line buffers
13	**Cur_RA<1>**	
14	**Cur_BUF<0>**	These 2 bits manage the current of the SCA output buffers
15	**Cur_BUF<1>**	

Table 10: Description of the register 2.

- ***bits Debug0 to Debug1***

These 2 bits allow the user to visualize on an oscilloscope the outputs of the CSA, PZC filter and Gain-2 from the channel number 1. Depending on these bits (see Table 11) , one among these outputs is multiplexed toward the ***Out_debug*** pad [pin N° 46] via an internal buffer.

Debug1	Debug0	Out_debug (canal1)
0	**0**	***Standby***
0	**1**	***CSA***
1	**0**	***CR***
1	**1**	***Gain2***

Table 11: Selection of the output in the "spy" mode.

- **read_from_0; test_digout; set_l0_when_rst; en_mker_rst; rst_lv_to 1.**

These 5 bits act directly on the readout of the SCA and will be used essentially for the test of the asic and FEC prototypes.

read_from_0: In the normal mode, the readout starts from the column following the last written. Set this bit to “1”, forces to start the readout from the physical column **0**.
test_digout: if “1”, a test pattern (“10101100”) is serialized to the output instead of the 9bit address of the last read column.
set_l0_when_rst: not used, for normal operation must be set to 0.
en_mker_rst: If “1”, a "digital" marker (near gnd or vdd levels) is multiplexed to the analog output during the first of the "reset states".
rst_lv_to 1: Set the level of the digital marker (when en_mker_rst=”1”). “0” means level near gnd; “1” means level near Vdd.

- **boost_pw.**

If 1, the output current of the GAIN-2 amplifier is increased by +20%. It can be used for very fast sampling frequencies and in case of chip fabricated in a “slow” corner process.

- **out_resync, synchro_inv & force_eout**

These 3 bits change some configurations for the Slow Control.
out_resync: If 1, the ***Sc_dout*** output data is resynchronized by a clock edge ***Sc_ck***, selected by ***synchro_inv***.
synchro_inv: Selects the edge for the synchronizing of the ***Sc_dout*** output data. “0” select the rising edge, “1” the falling.
force_eout: “1” inhibits the 3rd state functionality of the SC output buffer.

- ***bits*** **CUR_RA <1:0>**

These 2 bits are controlling the bias current of the 76 SCA line readout buffers. This control is also managed by the bits ***power_down_read*** & ***alternate_power*** of the register 1. The Table 12 gives the different values.

CUR_RA<1>	CUR_RA<0>	*power_down_read* & *alternate_power = “0”* I power	*power_down_read* or *alternate_power = “1”* I power
0	0	*211uA*	*172uA*
0	1	*274uA*	*211uA*
1	0	*395uA*	*274uA*
1	1	*735uA*	*395uA*

Table 12: Control of the SCA line buffer current.

The nominal configuration is: « **10** ».

- ***bits* CUR_BUF <1:0>**

These 2 bits are controlling the bias current of the group mux buffer of the 2 groups (one buffer for 38 lines) and also those of the final mux buffer. The Table 13 and Table 14 show the different values for the 2 kind of buffers.

CUR_BUF<1>	CUR_BUF<0>	I power on group mux buffer
0	0	*132uA*
0	1	*169uA*
1	0	*239uA*
1	1	*433uA*

Table 13: Control of the SCA group buffer current.

CUR_BUF<1>	CUR_BUF<0>	I power on final mux buffer
0	0	*482uA*
0	1	*620uA*
1	0	*831uA*
1	1	*1.610mA*

Table 14: Control of the SCA output buffer current.

The nominal configuration is: « **10** ».

6.8.C Injection Register 1.

This 38 bits register is located at address number 3. It is used to select the channel for the test (Table 15). The channel number goes from 1 to 36, and 1 to 2 for the FPN channel.

bit	name	action
0	**select_c36**	Selection of the channel 36 for the test
1	**select_c35**	Selection of the channel 35 for the test
2	**select_c34**	Selection of the channel 34 for the test
3	**select_c33**	Selection of the channel 33 for the test
4	**select_c32**	Selection of the channel 32 for the test
5	**select_c31**	Selection of the channel 31 for the test
6	**select_c30**	Selection of the channel 30 for the test
7	**select_c29**	Selection of the channel 29 for the test
8	**select_c28**	Selection of the channel 28 for the test
9	**select_c27**	Selection of the channel 27 for the test
10	**select_c26**	Selection of the channel 26 for the test
11	**select_c25**	Selection of the channel 25 for the test
12	**select_cfpn2**	Selection of the channel cfpn2 for the test
13	**select_c24**	Selection of the channel 24 for the test
14	**select_c23**	Selection of the channel 23 for the test
15	**select_c22**	Selection of the channel 22 for the test
16	**select_c21**	Selection of the channel 21 for the test
17	**select_c20**	Selection of the channel 20 for the test
18	**select_c19**	Selection of the channel 19 for the test
19	**select_c18**	Selection of the channel 18 for the test
20	**select_c17**	Selection of the channel 17 for the test
21	**select_c16**	Selection of the channel 16 for the test
22	**select_c15**	Selection of the channel 15 for the test
23	**select_c14**	Selection of the channel 14 for the test
24	**select_c13**	Selection of the channel 13 for the test
25	**select_cfpn1**	Selection of the channel cfpn1 for the test
26	**select_c12**	Selection of the channel 12 for the test
27	**select_c11**	Selection of the channel 11 for the test
28	**select_c10**	Selection of the channel 10 for the test
29	**select_c9**	Selection of the channel 9 for the test
30	**select_c8**	Selection of the channel 8 for the test
31	**select_c7**	Selection of the channel 7 for the test
32	**select_c6**	Selection of the channel 6 for the test
33	**select_c5**	Selection of the channel 5 for the test
34	**select_c4**	Selection of the channel 4 for the test
35	**select_c3**	Selection of the channel 3 for the test
36	**select_c2**	Selection of the channel 2 for the test
37	**select_c1**	Selection of the channel 1 for the test

Table 15: Description of the register 3.

6.8.D Injection Register 4

This 38 bits register is located at address number 4. It is used to select the channel for the test (Table 16). The channel number goes from 37 to 72, and 3 to 4 for the FPN channel.

bit	name	action
0	**select_c37**	Selection of the channel 37 for the test
1	**select_c38**	Selection of the channel 38 for the test
2	**select_c39**	Selection of the channel 39 for the test
3	**select_c40**	Selection of the channel 40 for the test
4	**select_c41**	Selection of the channel 41 for the test
5	**select_c42**	Selection of the channel 42 for the test
6	**select_c43**	Selection of the channel 43 for the test
7	**select_c44**	Selection of the channel 44 for the test
8	**select_c45**	Selection of the channel 45 for the test
9	**select_c46**	Selection of the channel 46 for the test
10	**select_c47**	Selection of the channel 47 for the test
11	**select_c48**	Selection of the channel 48 for the test
12	**select_cfpn3**	Selection of the channel cfpn3 for the test
13	**select_c49**	Selection of the channel 49 for the test
14	**select_c50**	Selection of the channel 50 for the test
15	**select_c51**	Selection of the channel 51 for the test
16	**select_c52**	Selection of the channel 52 for the test
17	**select_c53**	Selection of the channel 53 for the test
18	**select_c54**	Selection of the channel 54 for the test
19	**select_c55**	Selection of the channel 55 for the test
20	**select_c56**	Selection of the channel 56 for the test
21	**select_c57**	Selection of the channel 57 for the test
22	**select_c58**	Selection of the channel 58 for the test
23	**select_c59**	Selection of the channel 59 for the test
24	**select_c60**	Selection of the channel 60 for the test
25	**select_cfpn4**	Selection of the channel cfpn4 for the test
26	**select_c61**	Selection of the channel 61 for the test
27	**select_c62**	Selection of the channel 62 for the test
28	**select_c63**	Selection of the channel 63 for the test
29	**select_c64**	Selection of the channel 64 for the test
30	**select_c65**	Selection of the channel 65 for the test
31	**select_c66**	Selection of the channel 66 for the test
32	**select_c67**	Selection of the channel 67 for the test
33	**select_c68**	Selection of the channel 68 for the test
34	**select_c69**	Selection of the channel 69 for the test
35	**select_c70**	Selection of the channel 70 for the test
36	**select_c71**	Selection of the channel 71 for the test
37	**select_c72**	Selection of the channel 72 for the test

Table 16: Description of the register 4.

6.8.E Version number Register 6

This 16 bits register is located at address number 6. It contains the version number of the chip. For the production version, the version number is: 0X0101.

7 Power supply connections.

A significant number of pins of the AFTER chip (27 VDD + 30 GND) are dedicated to power supplies. The analog channels of AFTER are split into 2 groups of 38, for matching a square package. The height of these 2 groups (7mm) and the sensitivity of each block (CSA, CR, SK & G-2) imply to supply these blocks independently and homogeneous (Pins in top and bottom). This is also true for the SCA powering. The Fig 11 shows the internal architecture of the chip by indicating the placement and the name of the various building blocks.

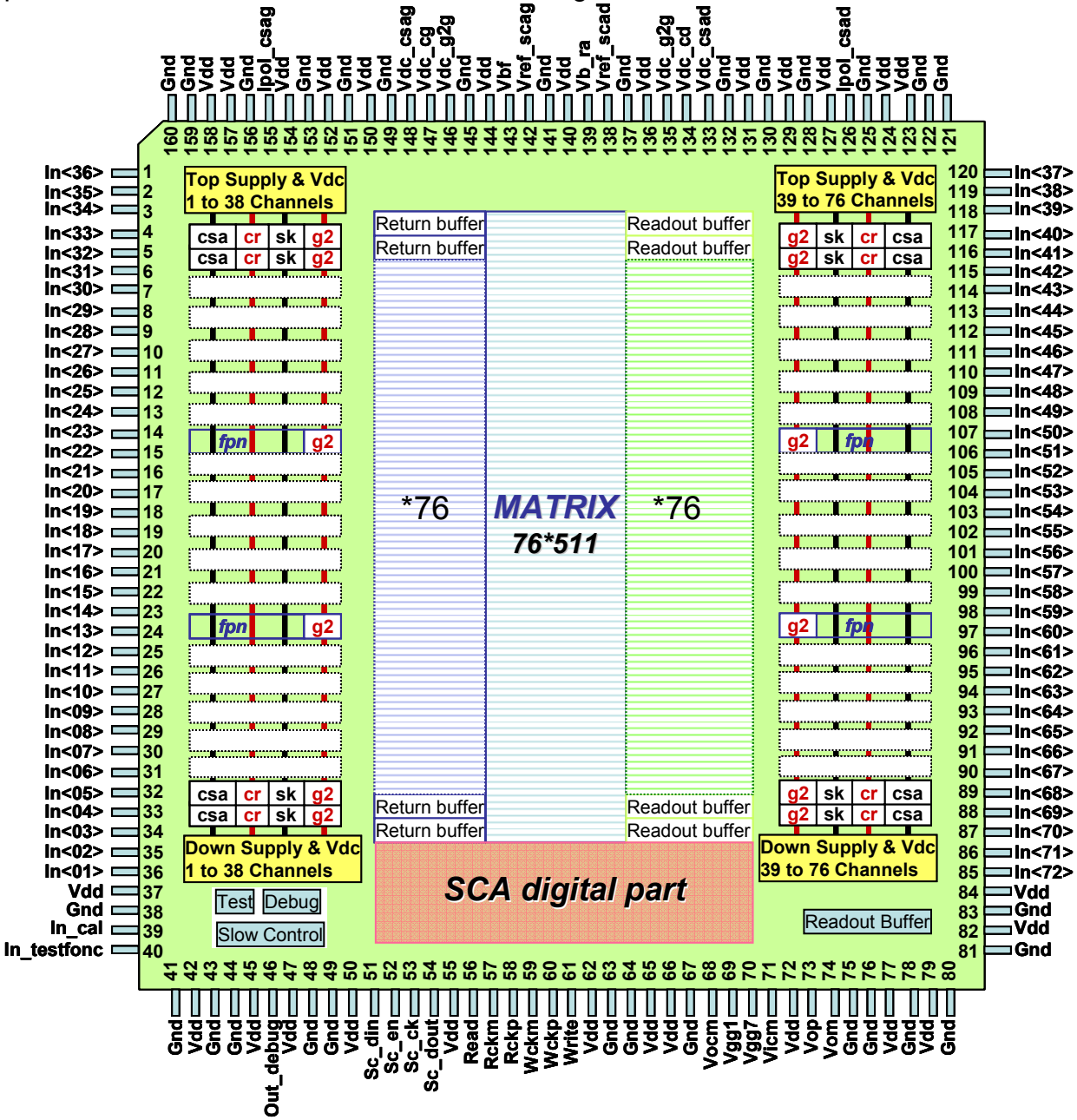


Fig 11: Internal architecture of AFTER.

7.1 *Cavity/leadframe connection.*

The substrat (P type) must be connected to the ground. This is done by connecting the bottom of the cavity with 4 pins (Fig 12).

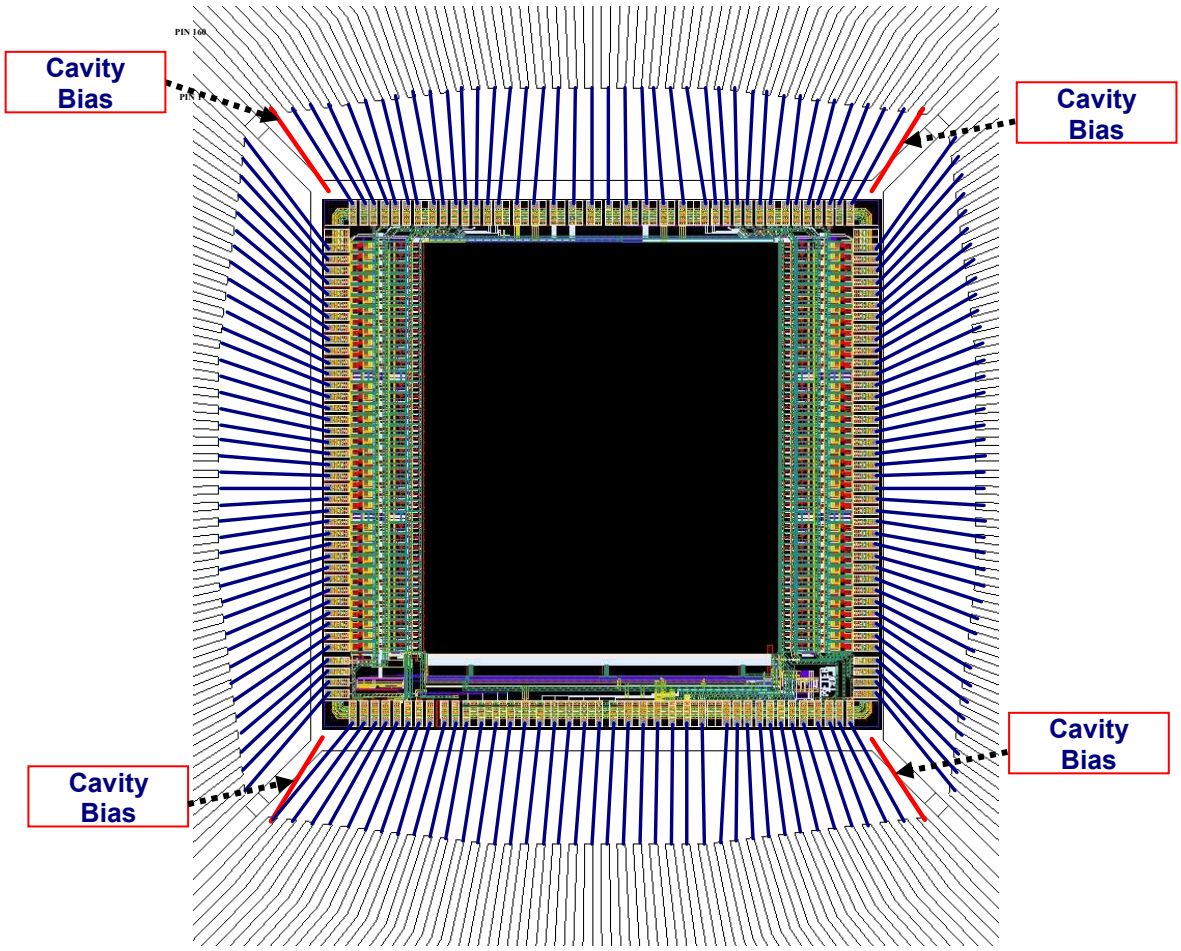


Fig 12: Bonding diagram of AFTER.

N° Pin	*Name*	*I dc*	*Description*
41	**Gnd_Substrat**	0A	Protection diode [37 to 84],cavity, SCA digital part guard ring & Slow Control
80	**Gnd_Substrat**	0A	Cavity
121	**Gnd_Substrat**	0A	Cavity
160	**Gnd_Substrat**	0A	Cavity

Table 17: Pins for the cavity connection.

The pin 41 is also used for:

- protection diodes of pins 37 to 84,
- guard ring of the digital part of the SCA,
- Slow Control.

7.2 *Protection diodes bias*

All the pins of the chip are protected by internal diodes. The power supplies of these diodes are carried out by independent pins, not used for the supply of internal blocks (except N° 55).

N° Pin	*Name*	*I dc*	*Description*
55	**Vdd_prob**	0A	Vdd for protection diode [37 to 84], SCA digital part guard ring & Slow Control
41	**Gnd_prob**	0A	Gnd for protection diode [37 to 84], SCA digital part guard ring & Slow Control
123	**Vdd_proind**	0A	Vdd for protection diode [37 to 72]:channels input
122	**Gnd_proind**	0A	Gnd for protection diode [37 to 72]:channels input
140	**Vdd_proh**	0A	Vdd for protection diode 124 to 157]
141	**Gnd_proh**	0A	Gnd for protection diode 124 to 157]
158	**Vdd_proing**	0A	Vdd for protection diode [1 to 36]:channels input
159	**Gnd_proing**	0A	Gnd for protection diode [1 to 36]:channels input

Table 18: Pins for the protection diodes bias.

7.3 *Analog channels bias.*

The front-end part of the analog channel is made of 4 blocks:

- CSA (Table 19),
- PZC block (Table 20),
- SK filter (Table 21),
- Gain -2 (Table 22).

Each of them uses dedicated pins for power supplies:

7.3.A CSA

N° Pin	*Name*	*I dc (mA)*	*Description*
37	**Vdd_csag**	2.43 + Ipol_csag*[1 + 18*(1+R_1b_0)]	**Vdd&Gnd for the CSA of the channel 36 to 1**
38	**Gnd_csag**	2.43 + Ipol_csag*[1 + 18*(1+R_1b_0)]	
157	**Vdd_csag**	2.43 + Ipol_csag*[1 + 18*(1+R_1b_0)]	
156	**Gnd_csag**	2.43 + Ipol_csag*[1 + 18*(1+R_1b_0)]	
84	**Vdd_csad**	2.43 + Ipol_csad*[1 + 18*(1+R_1b_0)]	**Vdd&Gnd for the CSA of the channel 37 to 72**
83	**Gnd_csad**	2.43 + Ipol_csad*[1 + 18*(1+R_1b_0)]	
124	**Vdd_csad**	2.43 + Ipol_csad*[1 + 18*(1+R_1b_0)]	
125	**Gnd_csad**	2.43 + Ipol_csad*[1 + 18*(1+R_1b_0)]	

Table 19: CSA power supplies.

The d.c power consumption current depends on 2 parameters:

- The value of CSA nominal bias current set externally on the FEC by resistors connected to the pins Ipol_csag (N° 155) / Ipol_csad (N° 124) :
- The sate of the bit#0 of the register 1 (see Table 6). If it is 1: the CSA bias current is doubled, if it is 0, the nominal bias current is used.

7.3.B Pole-zero Stage.

N° Pin	Name	I dc	I dc (power down)	Description
42	Vdd_crg	3.9mA	1.1mA	Vdd&Gnd for the PZC of the channel 36 to 1
43	Gnd_crg	3.9mA	1.1mA	
154	Vdd_crg	3.9mA	1.1mA	
153	Gnd_crg	3.9mA	1.1mA	
82	Vdd_crd	3.9mA	1.1mA	Vdd&Gnd for the PZC of the channel 37 to 72
81	Gnd_crd	3.9mA	1.1mA	
127	Vdd_crd	3.9mA	1.1mA	
128	Gnd_crd	3.9mA	1.1mA	

Table 20: PZ supply power supplies.

7.3.C SK filter

N° Pin	Name	I dc	I dc (power down)	Description
45	Vdd_skg	1.9mA	740uA	Vdd&Gnd for the SK of the channel 36 to 1
44	Gnd_skg	1.9mA	740uA	
152	Vdd_skg	1.9mA	740uA	
151	Gnd_skg	1.9mA	740uA	
79	Vdd_skd	1.9mA	740uA	Vdd&Gnd for the SK of the channel 37 to 72
78	Gnd_skd	1.9mA	740uA	
129	Vdd_skd	1.9mA	740uA	
130	Gnd_skd	1.9mA	740uA	

Table 21: SK filter power supplies

7.3.D x2 Gain

N° Pin	Name	I dc	I dc (power down)	Description
47	Vdd_g2g	6.881mA	1.73mA	Vdd&Gnd for the Gain-2 of the channel 36 to 1 + 2 FPN
48	Gnd_g2g	6.881mA	1.73mA	
150	Vdd_g2g	6.881mA	1.73mA	
149	Gnd_g2g	6.881mA	1.73mA	
77	Vdd_g2d	6.881mA	1.73mA	Vdd&Gnd for the Gain-2 of the channel 37 to 72 + 2FPN
76	Gnd_g2d	6.881mA	1.73mA	
131	Vdd_g2d	6.881mA	1.73mA	
132	Gnd_g2d	6.881mA	1.73mA	

Table 22:2x Gain power supplies.

7.4 SCA power supplies

The SCA is divided into 4 parts:

- The matrix [511*76 analog cells],
- The input stage “return buffers” [1 per line] (Table 23),
- The SCA read amplifiers [1 per line] (Table 24),
- The digital part [clock, address …] (Table 25).

7.4.A The analog memory cell matrix

The supply of the matrix is made by a metal grid on its entire surface. This grid is connected to the power bus supply of the return buffer and of the output. The D.C power consumption of this part is zero.

7.4.B The «return buffer» amplifiers.

This stage buffers the V_{return} voltage, defined outside by the pad **142** (Vref_scag), to provide it as a reference to the memory cells.

N° Pin	*Name*	*I dc*	*Description*
50	**Vdd**	3.676mA	**Vdd&Gnd for the “buffer return” & Matrix**
49	**Gnd**	3.676mA	
144	**Vdd**	3.676mA	
145	**Gnd**	3.676mA	

Table 23: Power supplies of the «return buffer».

7.4.C The SCA read amplifiers

This amplifier is used to read back the analog data stored in the memory cells. It is active only during the read phase. Its power consumption value is adjustable by slow control.

N° Pin	*Name*	*I dc*	*Description*
66	**Vdd**	6.62mA	**Vdd&Gnd for the SCA readout Amplifier & Matrix (configuration: Cur_RA<1>: “1”; Cur_RA<0>:”0” and Power_down_write: “0”)** (nominal config)
67	**Gnd**	6.62mA	
136	**Vdd**	6.62mA	
137	**Gnd**	6.62mA	

Table 24: Power supplies of SCA line buffer.

7.4.D Digital part

This part generates and distributes the signals required for the writing & reading operations in the SCA. Its DC power consumption is 0, excepted for the LVDS input buffers.

N° Pin	*Name*	*I dc*	*Description*
62	**Vdd**	343.3uA	**Vdd&Gnd for the LVDS receivers & CSA write clock block**
63	**Gnd**	343.3uA	
65	**Vdd**	0mA	**Vdd&Gnd for the CSA logic part**
64	**Gnd**	0mA	

Table 25: Power supplies of the digital part.

7.5 *Output multiplexer and output buffer.*

This section of the chip includes the analog output multiplexer and the differential output buffer.

N° Pin	*Name*	*I dc*	*Description*
72	Vdd_out	16.03mA (15mA from differential output buffer)	Vdd&Gnd for the Readout buffer & SCA group buffers (configuration: Vgg1=2mA&Vgg7=1mA)
75	Gnd	16.03mA (15mA from differential output buffer)	

Table 26: Power supplies of the output buffers.

8 The D.C voltage and current references

8.1 *The D.C voltage references*

Some DC reference voltages used in the AFTER chip have to be defined externally. These voltages can be adapted to the signal polarity in order to maximize the chip dynamic range.
These voltages are:

- The CSA DC output voltage,
- The PZ & SK filter DC output voltages,
- The x2 Gain DC output voltage,
- The Gain-2 & SCA DC reference voltages,
- The differential output buffer DC input & output voltages.

Excepted for the reference voltage defining the input common mode voltage of the output buffer, the input pads associated to these reference have high DC input impedance (>10 Mohm). Therefore, the reference voltages, defined on the ***FEC***, could be derived from the power supply by low power consumption resistor bridges as shown in the Fig 13. For high frequency noise reduction, the voltage references must be bypassed to ground by 100nF ceramic capacitors.

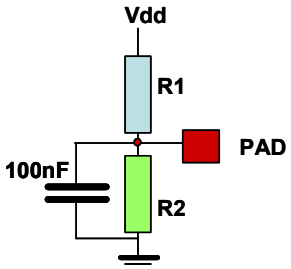


Fig 13: Example of an external reference voltage.

8.1.A CSA DC output voltage.

N° Pin	*Name*	*Vdc*	*I dc*	*Description*
133	Vdc_csad	*2V (+/- 2%)*	*0mA*	*d.c output level voltage of the CSA [37 to 72]*
148	Vdc_csag	*2V (+/- 2%)*	*0mA*	*d.c output level voltage of the CSA [36 to 1]*

Table 27: Pins setting the CSA DC output voltages.

8.1.B PZ & SK filter DC output voltages.

N° Pin	Name	Vdc	I dc	Description
134	Vdc_cd	2.2V (+/- 2%)	0mA	d.c output level voltage of the PZC & SK filter [37 to 72]
147	Vdc_cg	2.2V (+/- 2%)	0mA	d.c output level voltage of the PZC & SK filter [36 to 1]

Table 28: Pins setting the PZ & SK filters DC output voltages.

The AFTER chip is able to treat anode (TPC of T2K) or cathode polarity signals. To maximize the analog chain dynamic range, different reference voltages will be used depending on the signal polarity: 2.2V for the anode polarity.; 0.7V for the cathode polarity.

8.1.C x2-Gain DC output voltage.

N° Pin	Name	Vdc	I dc	Description
135	Vdc_g2d	0.7V (+/- 2%)	0mA	d.c output level voltage of the Gain-2 [37 to 72]
146	Vdc_g2g	0.7V (+/- 2%)	0mA	d.c output level voltage of the Gain-2 [36 to 1]

Table 29: Pins setting the x2 Gain stage DC output voltage.

The optimum voltage is: 0.7V for the anode polarity; 2.2V for the cathode polarity.

8.1.D Reference voltages of the x2 Gain and the SCA

N° Pin	Name	Vdc	I dc	Description
138	Vref_scad	0.7V (+/- 2%)	0mA	d.c input level voltage of the Gain-2 [37 to 72] & reference voltage of the memory cells (Vreturn)
142	Vref_scag	0.7V (+/- 2%)	0mA	d.c input level voltage of the Gain-2 [36 to 1] & reference voltage of the memory cells (Vreturn)

Table 30: x2 Gain stage & SCA reference voltages.

The absolute value of these voltages is not critical. But they must be larger than 0.6V and smaller than 1.5V. The two voltages must be equal.

8.1.E DC input common mode voltage of the differential output buffer

N° Pin	Name	Vdc	I dc	Description
71	Vicm	1.45V (+/- 2%)	[Vop – Vicm]/11.638KΩ	Input Common mode voltage for readout buffer

Table 31: DC input common mode voltage of the differential output buffer.

Unlike the other reference voltages, and because it drives a quite low impedance node, the voltage source providing this voltage must be able to sink or source a current in a range of - 26uA to +60uA. Moreover, its impedance should be smaller than few 10Ω to avoid non-linearity.

8.1.F Common mode output voltage of the output buffer

N° Pin	Name	Vdc	I dc	Description
68	Vocm	VddADC/2	0mA	Output common mode voltage of the readout buffer

Table 32: common mode output voltage of the differential output buffer.

8.2 *The D.C current references.*

Some bias currents used by the AFTER chip must be defined externally on the FEC. This is the case for those of:

- the CSA input transistor,
- the input & output stages of the output buffer.

All these currents can be defined using resistor connected between the bias pad and the ground like on Fig 14. Inside the chip, a PMOS transistor, with source connected to vdd and with the gate and the drain connected to the pad is defining the bias current. For optimum noise performances, the pad voltage should be bypassed to the vdd used to supply the block biased by the reference.

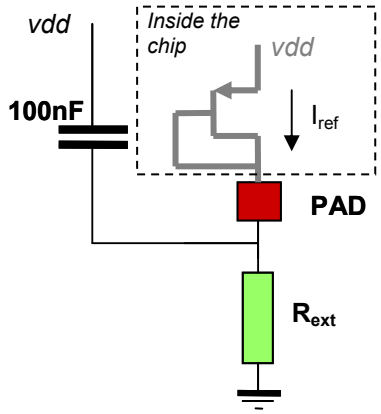


Fig 14: Principle of external bias current reference.

8.2.A Input transistor bias current of the CSA

N° Pin	*Name*	*I dc*	*Description*
126	Ipol_csad	*note*	*Current supply of the CSA input transistor [37 to 72]*
155	Ipol_csag	*note*	*Current supply of the CSA input transistor [36 to 1]*

Table 33: Pins for reference current of the CSA.

This current value can be tuned to optimize the noise. The tuning range extends from 200uA to 1mA. A R_{ext} resistor of 5.1K set the bias current of the CSA to 400µA (or 800µA if the slow control bit doubling this current is set).

8.2.B Input & output stage bias currents of the output buffer.

N° Pin	*Name*	*I dc*	*resistor to gnd nominal value*	*Description*
69	Vgg1	*2mA*	*1.24K*	*Current bias of the input stage of the Readout buffer*
70	Vgg7	*1mA*	*2K*	*Current bias of the output stage of the Readout buffer*

Table 34: Pins setting the input & output bias currents of the output buffer.

These values are the best one to optimize the buffer settling time when loaded by the ADC.

9 Typical performance characteristics

The main performances of the AFTER asic are reported in the Table 35.

Parameter					Unit	Condition
Power consumption				446 / 540	*mW*	*Icsa: 400 µA / 800µA;Vdd:3.3V*
Transfer Function						
120 fC				18	*mV / fC*	*Icsa: 800µA;* *Peaking Time: 100ns;* *Fsampling: 50 MHz;* *Cin: 22 pF*
240 fC				9.7	*mV / fC*	
360 fC				6.67	*mV / fC*	
600 fC				4.1	*mV / fC*	
Output voltage range (differential)				2	*V p-p*	
Integral Nonlinearity						Fsampling < 100 MHz
				< 1.2	%	Peaking Time = 100 ns
				< 0.5	%	Peaking Time = 2 µs
Crosstalk						
				< +/- 0.4	%	
Signal shape	Tpeak		Tfall	Tfwhm		
100 ns	111		182	150	*ns*	Tpeak: signal rise time [5% full amplitude / peak] Tfall: signal fall time [peak / 5% full amplitude] Tfwhm: signal width [50% full amplitude]
200 ns	185		552	287	*ns*	
400 ns	387		823	631	*ns*	
1000 ns	893		2118	1529	*ns*	
2000 ns	1776		4037	2953	*ns*	
Baseline spread						
				78 to 146	*mV p-p*	
Noise	Peaking Time (ns)					
	100	200	500	2000		
120 fC						Linear parameterization (Valid for 15 pF – 40 pF input capacitance range). Icsa: 800 µA
Offset	350	370	415	404	*e-*	
Slope	22.2	14.6	7.8	5.3	*e- / pF*	
240 fC						
Offset	690	700	775	750	*e-*	
Slope	13	8.5	4.5	3.1	*e- / pF*	
360 fC						
Offset	1015	1050	1135	1092	*e-*	
Slope	10.7	5.6	3	2.8	*e- / pF*	
600 fC						
Offset	1700	1740	1817	1780	*e-*	
Slope	6.5	3.2	3.3	1.8	*e- / pF*	

Table 35: Typical performance characteristics of the AFTER chip.

10 AFTER chip Pinout.

The AFTER chip is packaged in a 160-pin Low Quad Flat Pack (LQFP-160). The package body dimensions are 28 x 28 x 1.4 mm. Its pitch is 0.65mm with a 2 mm footprint. The analog inputs are divided into two groups of 36 located each on one side of the package. This arrangement has been chosen to avoid fine pitch bonding or long and large angles bonding.
The pinout of the AFTER chip is given in the Fig 15 and the Table 36.

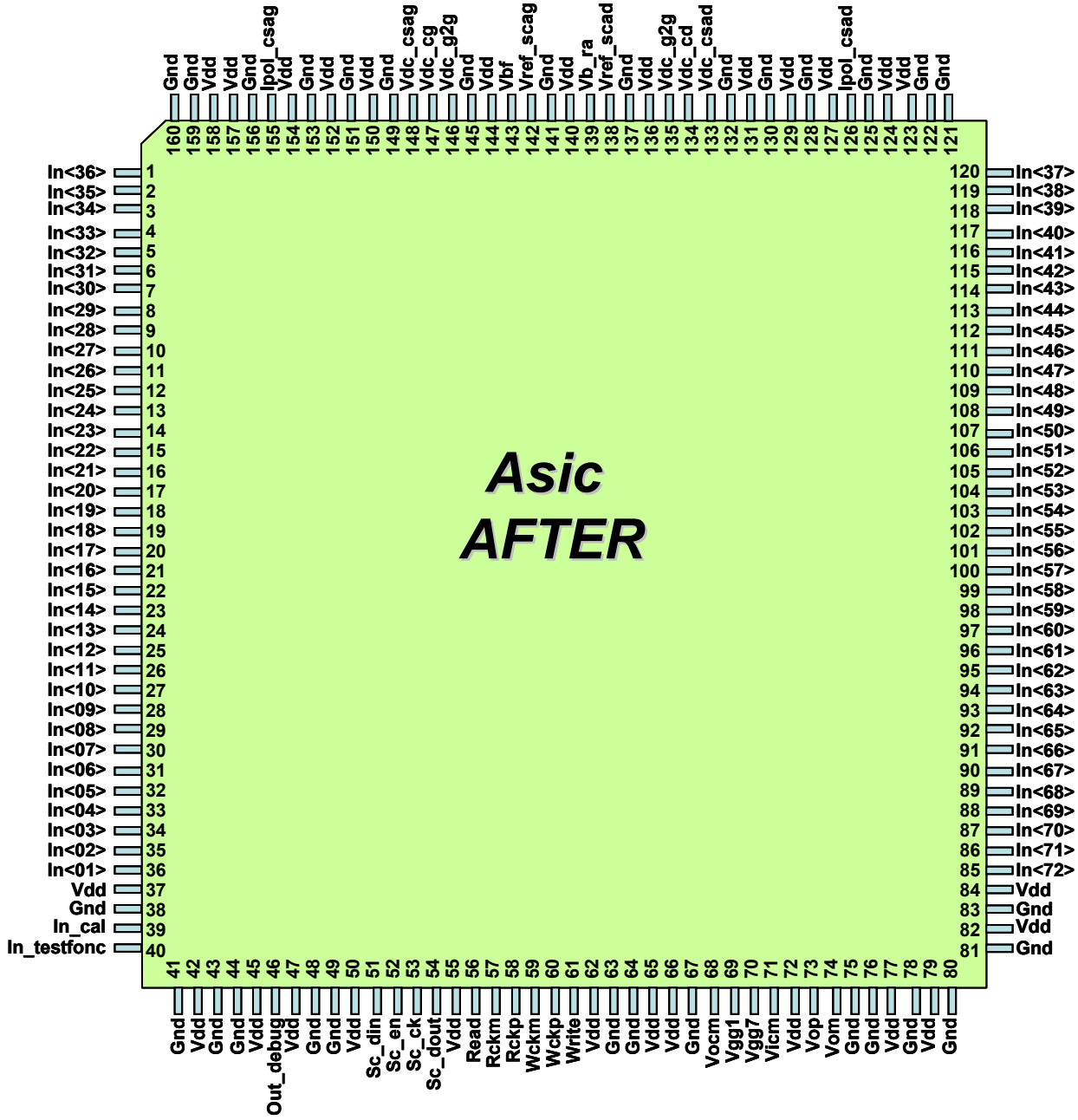


Fig 15: Pinout of the packaged AFTER chip.

N° Pin	Name	Dir.	Level	Description
1 to 36	In<36> to In<1>	In	Analog	Inputs of channels 36 to 1
37	Vdd_csag	In	3.3V	Vdd for the csa of the channels 36 to 1
38	gnd	In	0V	Gnd for the csa of the channels 36 to 1
39	In_cal	In	Analog	Input for the calibration
40	In_testfonc	In	Analog	Input for the test & functionality
41	gnd	In	0V	Gnd for protection diode [37 to 84]., cavity , SCA digital part guard ring & Slow Control
42	Vdd_crg	In	3.3V	Vdd for the PZC of the channels 36 to 1
43	gnd	In	0V	Gnd for the PZC filter of the channels 36 to 1
44	gnd	In	0V	Gnd for the SK filter of the channels 36 to 1
45	Vdd_skg	In	3.3V	Vdd for the SK filter of the channels 36 to 1
46	Out_debug	Out	Analog	Output of the “spy” mode
47	Vdd_g2g	In	3.3V	Vdd for the Gain -2 of the channels 36 to 1
48	gnd	In	0V	Gnd for the Gain -2 of the channels 36 to 1
49	gnd	In	0V	Gnd return buffer + Matrix
50	vdd	In	3.3V	Vdd return buffer + Matrix
51	Sc_din	In	CMOS 3.3V	Serial data input of Slow Control
52	Sc_en	In	CMOS 3.3V	Chip Select input of Slow Control
53	Sc_ck	In	CMOS 3.3V	Serial clock input of Slow Control
54	Sc_dout	Out	CMOS 3.3V	Serial data output of Slow Control
55	Vdd_prob	In	3.3V	Vdd for protection diode [37 to 84], SCA digital part guard ring & Slow Control
56	read	In	CMOS 3.3V	SCA read mode
57	rckm	In	LVDS	SCA Negative read clock
58	rckp	In	LVDS	SCA Positive read clock
59	wckm	In	LVDS	SCA Negative write clock
60	wckp	In	LVDS	SCA Positive write clock
61	write	In	CMOS 3.3V	SCA write mode
62	vdd	In	3.3V	Vdd LVDS receiver & block SCA Write Clock
63	gnd	In	0V	Gnd LVDS receiver & block SCA Write Clock
64	gnd	In	0V	Gnd SCA logic
65	vdd	In	3.3V	Vdd SCA logic
66	vdd	In	3.3V	Vdd SCA Readout Amplifier + Matrix
67	gnd	In	0V	Gnd SCA Readout Amplifier + Matrix
68	vocm	In	VddADC/2	Common mode output voltage of the Readout buffer
69	Vgg1	Out	Current 2mA	Current bias of the input stage of Readout buffer
70	Vgg7	Out	Current 1mA	Current bias of the output stage of Readout buffer
71	vicm	In	1.45V mean	Common mode input voltage of the Readout buffer
72	Vdd_out	In	3.3V	Vdd of the Readout buffer & SCA buffer
73	vop	Out	Analog	Positive output of the Readout buffer
74	vom	Out	Analog	Negative output of the Readout buffer
75	gnd	In	0V	Gnd buffer out + logic
76	gnd	In	0V	Gnd for the Gain -2 of the channels 37 to 72
77	Vdd_g2d	In	3.3V	Vdd for the Gain -2 of the channels 37 to 72
78	gnd	In	0V	Gnd for the SK filter of the channels 37 to 72
79	Vdd_skd	In	3.3V	Vdd for the SK filter of the channels 37 to 72
80	gnd	In	0V	Gnd for cavity

N° Pin	Name	Dir.	Level	Description
81	gnd	In	0V	Gnd for the PZC filter of the channels 37 to 72
82	Vdd_crd	In	3.3V	Vdd for the PZC filter of the channels 37 to 72
83	gnd	In	0V	Gnd for the CSA of the channels 37 to 72
84	Vdd_csad	In	3.3V	Vdd for the CSA of the channels 37 to 72
85 to 120	In<72> to In<37>	In	Analog	Inputs of channels 72 to 37
121	gnd	In	0V	Gnd for cavity
122	gnd	In	0V	Gnd for protection diode [37 to 72]
123	Vdd_proind	In	3.3V	Vdd for protection diode [37 to 72]
124	Vdd_csad	In	3.3V	Vdd for the CSA of the channels 37 to 72
125	gnd	In	0V	Gnd for the CSA of the channels 37 to 72
126	Ipol_csad	Out	Current	Current supply of the input transistors of CSA [37 to 72]
127	Vdd_crd	In	3.3V	Vdd for the PZC of the channels 37 to 72
128	gnd	In	0V	Gnd for the PZC of the channels 37 to 72
129	Vdd_skd	In	3.3V	Vdd for the SK filter of the channels 37 to 72
130	gnd	In	0V	Gnd for the SK filter of the channels 37 to 72
131	Vdd_g2d	In	3.3V	Vdd for the Gain -2 of the channels 37 to 72
132	gnd	In	0V	Gnd for the Gain -2 of the channels 37 to 72
133	Vdc_csad	In	2V typ.	d.c output level voltage of the CSA [37 to 72]
134	Vdc_cd	In	2.2V [0.7V]	d.c output level voltage of the PZC & SK filter [37 to 72]
135	Vdc_g2d	In	0.7V [2.2V]	d.c output level voltage of the Gain -2 [37 to 72]
136	Vdd	In	3.3V	Vdd SCA Readout Amplifier + Matrix
137	gnd	In	0V	Gnd SCA Readout Amplifier + Matrix
138	vref_scad	In	0.7V	d.c reference level voltage of the SCA
139	vb_ra	in/out	analog	Current source voltage of the internal readout buffer; Control purpose
140	vdd_proh	In	3.3V	Vdd for protection diode [124 to 157]
141	gnd	In	0V	Gnd for protection diode [124 to 157]
142	vref_scag	In	0.7V	d.c reference level voltage of the SCA
143	vbf	in/out	analog	Current source voltage of the Matrix return bus
144	Vdd	In	3.3V	Vdd return buffer + Matrix
145	gnd	In	0V	Gnd return buffer + Matrix
146	Vdc_g2g	In	0.7V [2.2V]	d.c output level voltage of the Gain -2 [36 to 1]
147	Vdc_cg	In	2.2V [0.7V]	d.c output level voltage of the PZC & SK filter [36 to 1]
148	Vdc_csag	In	2V typ.	d.c output level voltage of the CSA [36 to 1]
149	gnd	In	0V	Gnd for the Gain 2 of the channels 36 to 1
150	Vdd_g2g	In	3.3V	Vdd for the Gain 2 of the channels 36 to 1
151	gnd	In	0V	Gnd for the SK filter of the channels 36 to 1
152	Vdd_skg	In	3.3V	Vdd for the SK filter of the channels 36 to 1
153	gnd	In	0V	Gnd for the PZC of the channels 36 to 1
154	Vdd_crg	In	3.3V	Vdd for the PZC filter of the channels 36 to 1
155	Ipol_csag	in/out	Current	Current supply of the input transistors of CSA [36 to 1]
156	gnd	In	0V	Gnd for the CSA of the channels 36 to 1
157	Vdd_csag	In	3.3V	Vdd for the CSA of the channels 36 to 1
158	Vdd_proing	In	3.3V	Vdd for protection diode [36 to 1]
159	gnd	In	0V	Gnd for protection diode [36 to 1]
160	gnd	In	0V	Gnd for cavity

Table 36: After pinout description.

11 Digital Input/Output Specifications.

The AFTER chip makes use of two kinds of digital input/ouput signals: CMOS and LVDS.
The CMOS signals are unipolar signals whereas “LVDS” signals are differential. The “LVDS” inputs are compatible with LVDS levels but also with other differential standard (like PECL). For LVDS signals, the suffix “p” is for the positive signal phase and “m” for the negative one. The digital signal is defined as the difference between the positive and negative phases.

Nom	Description	Min	Typ.	Max
VDD	Power supply voltage	3.2V	3.3V	3.4V
Vcmm LVDSin	Mode commun LVDS en entrée	0.6V	1.2 V	VDD-0.3V
Vswing LVDSin	input swing for LVDS inputs	0.2V	0.4 V	3.3V (1)
VCMOSin_l	low CMOS input level	VSS-0.2V	0	0.8V
VCMOSin_h	High CMOS input level	VDD-0.8V	VDD	VDD + 0.2V
Rin_dig	Input impedance for digital inputs	10 MOhm		
RinCMOS	Input resitance of CMOS input	10MOhm		
RinLVDSin	input resistance of LVDS	10MOhm		
RdifLVDSin	Différential input resistance of LVDS diff. input	10MOhm (2)		
Cin_ding	Input capacitor of digital inputs		4pF	
VCMOSout_l	Low CMOS output level	0		+0.4V
VCMOSout_h	High CMOS ouput level	VDD-0.4V		VDD
ICMOSout	Curent deliverable by CMOS output			4 mA

Table 37: Main specifications for AFTER digital input/ouputs.

(1) Even, if they are also compatible with largest swing signal, it is better to use them with small swing digital signal for noise reason.
(2) There is no 100 Ohm resistor integrated between the two pins of a LVDS differential input inside the chip.

12 Chip Layout.

The integrated circuit is manufactured using the AMS CMOS 0.35 µm technology. The die area is 7800 µm x 7400 µm for 500,000 transistors used. The number of pads is 160.

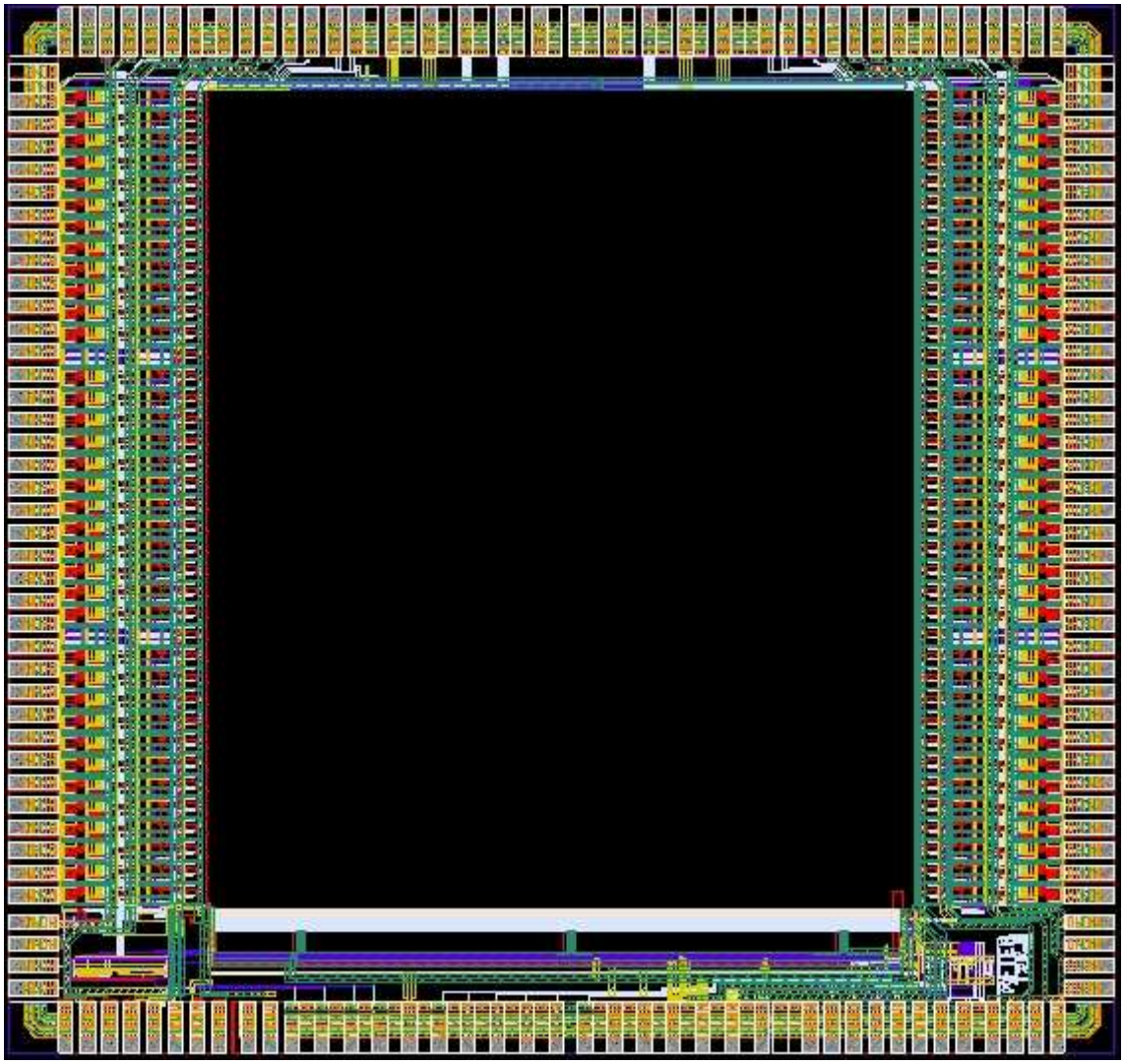
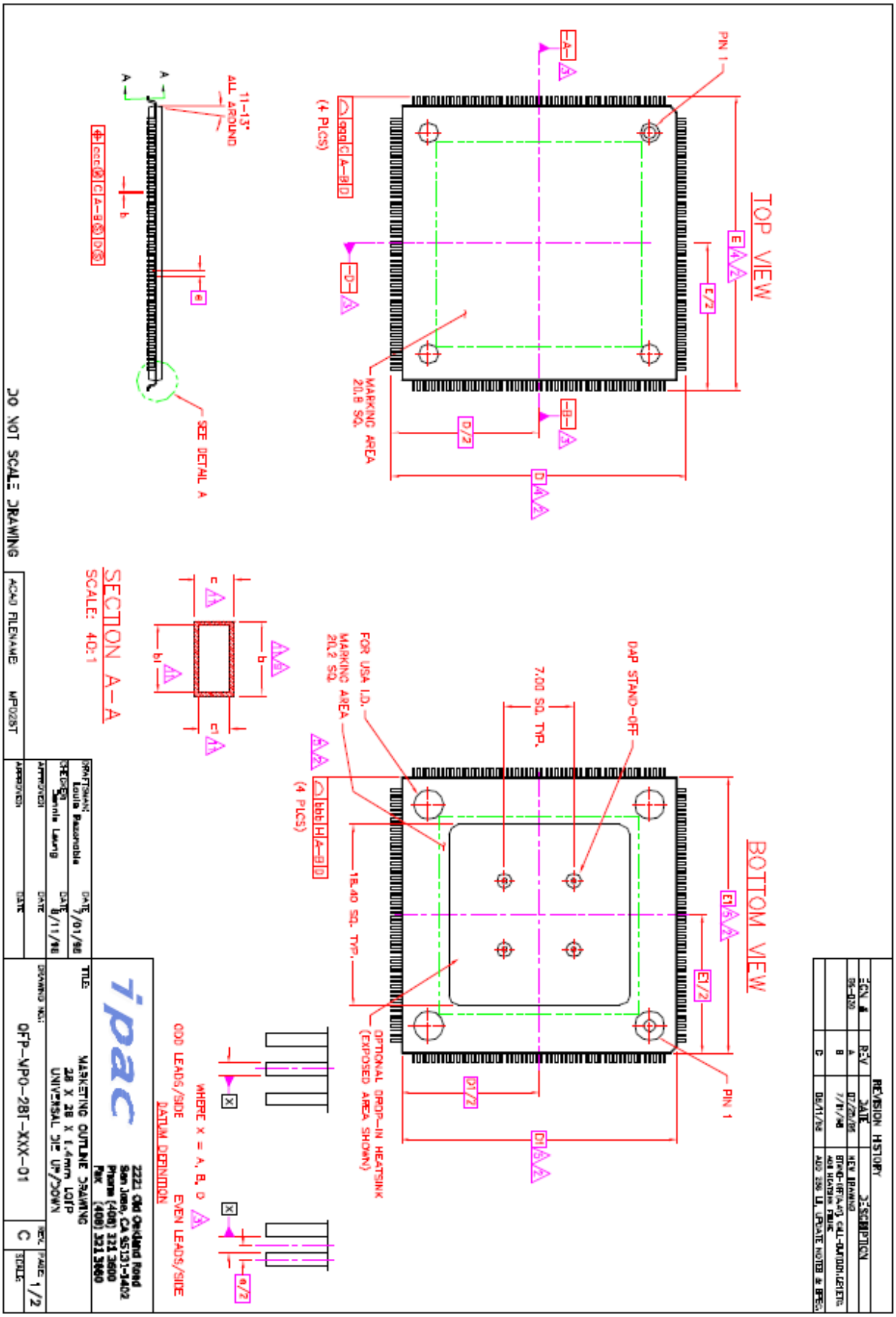
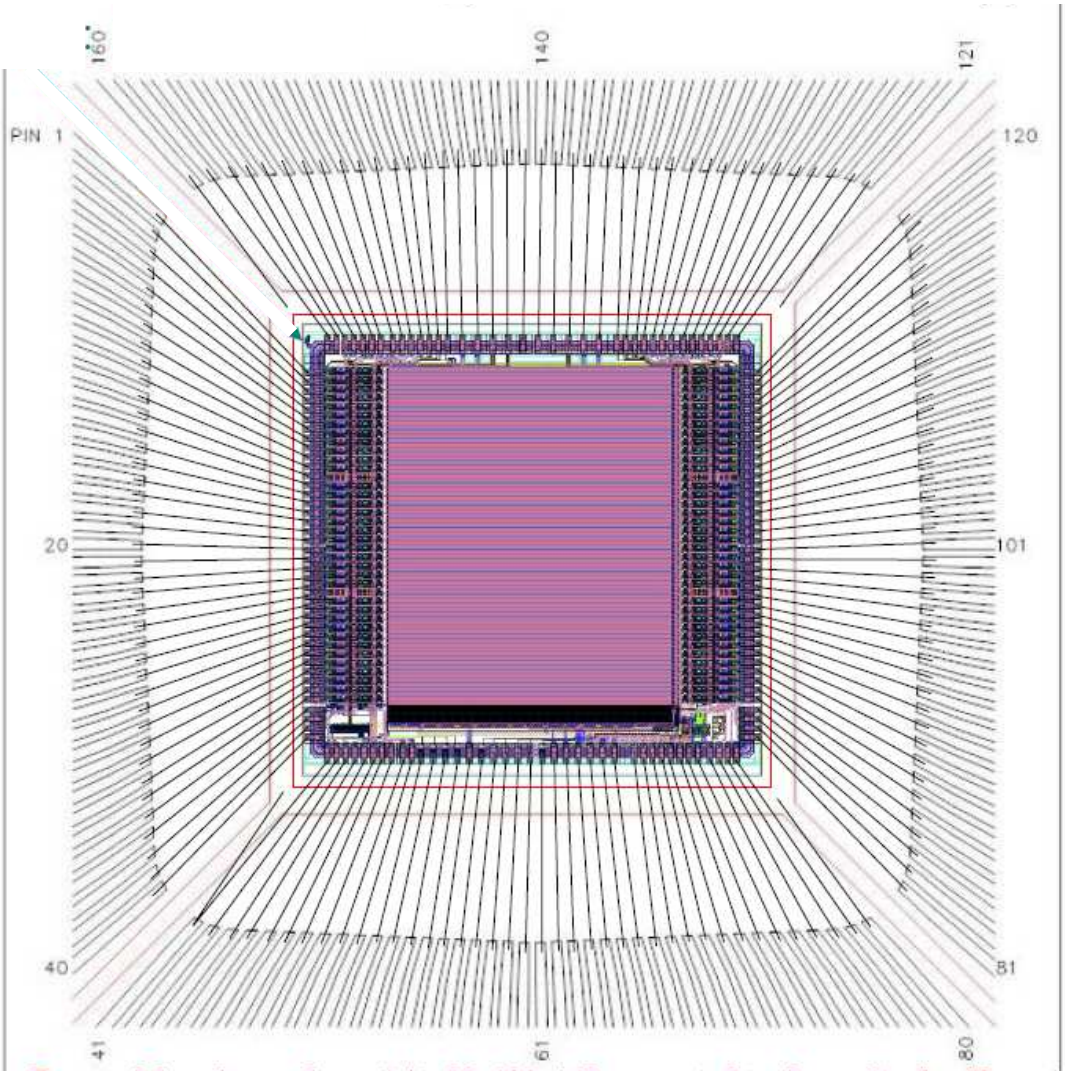


Fig 16: Layout of the AFTER chip

ANNEXE 1: Package Description.


TOP VIEW
BOTTOM VIEW
SECTION A-A
SCALE: 4O:1
SEE DETAIL A
MARKING AREA
DAP STAND-OFF
OPTIONAL DROP-IN HEATSINK
(EXPOSED AREA SHOWN)
EVEN LEADS/SIDE
ODD LEADS/SIDE
DATUM DEFINITION
DO NOT SCALE DRAWING
QFP-VPO-28T-XXX-01
MARKETING OUTLINE DRAWING
28 X 28 X 1.4mm LQFP
UNIVERSAL SIZ UP/DOWN
2221 Old Oakland Road
San Jose, CA 95131-1402
Phone (408) 321 3600
Fax (408) 321 3660
REVISION HISTORY

ANNEXE 2: Bonding Diagram of the AFTER chip.



Be careful: - pins package # 41, 80, 121, 160 connected to the cavity (leadframe)
- double bonding on pin package #41

√ CHECK PIN 1 DIE ORIENTATION WITH RESPECT TO WAFER FLAT

ECN#	REV.	DESCRIPTION	DATE		
98-121	A	NEW RELEASE	04/28/98	DRAWN:	DATE:
00-155	B	CHANGED SCALE TO 1:1	08/08/00	CHECKED:	DATE
				APPROVED:	DATE
				APPROVED:	DATE
				DWG. NUMBER: QFP-80-2850-160-01	

LEADFRAME: LF1-A160-202

D/A PAD SIZE: 7.6mm X 7.6mm

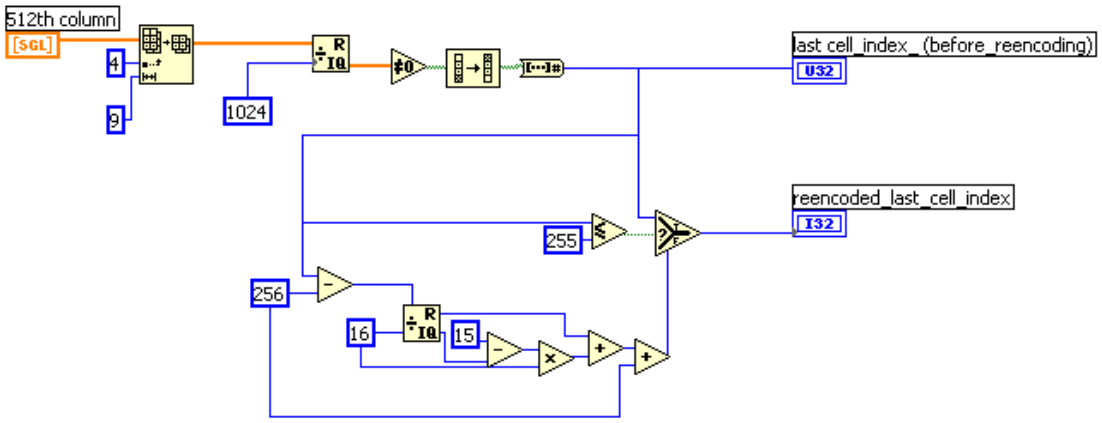
SCALE: DO NOT SCALE DRAWING

BOND SHELL – 28 x 28 x 1.4 LQFP. 160 LD

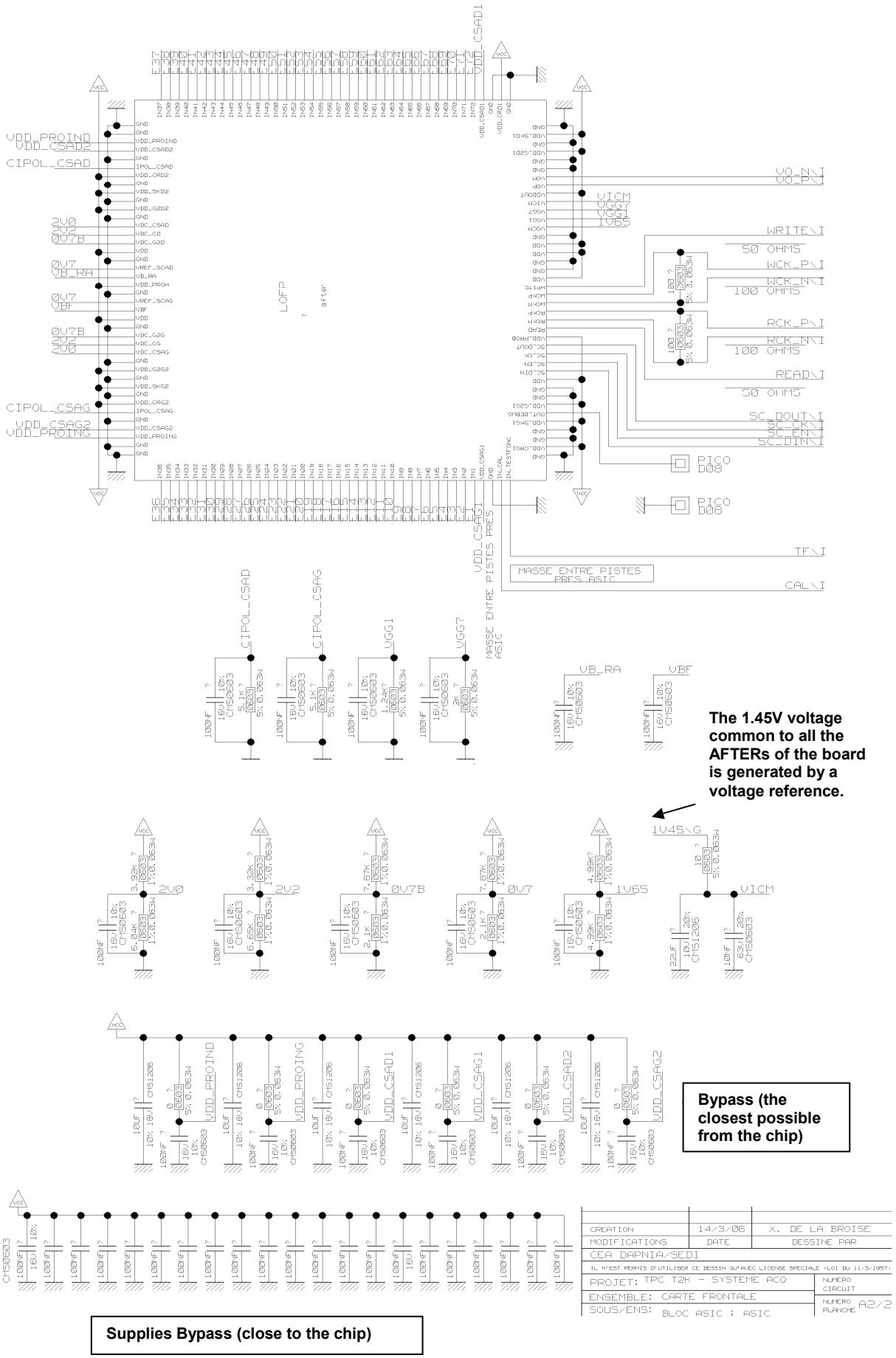
ipac

2221 Old Oakland Road
San Jose, CA 95131-1402
Phone (408) 321 3600

ANNEXE 3: Labview vi to correct encoding of the “last read cell” information in the prototype version of the chip.



ANNEXE 4: Schematic of the AFTER implementation in the FEC of T2K.



The 1.45V voltage common to all the AFTERs of the board is generated by a voltage reference.

Bypass (the closest possible from the chip)

Supplies Bypass (close to the chip)

CREATION	14/3/06	X. DE LA BROISE
MODIFICATIONS	DATE	DESSINE PAR
CEA DAPNIA/SEDI		
IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957)		
PROJET: TPC T2K - SYSTEME ACQ		NUMERO CIRCUIT
ENSEMBLE: CARTE FRONTALE		NUMERO PLANCHE A2/2
SOUS/ENS: BLOC ASIC ; ASIC		